Latest status of SAMPA v5 in sPHENIX TPC

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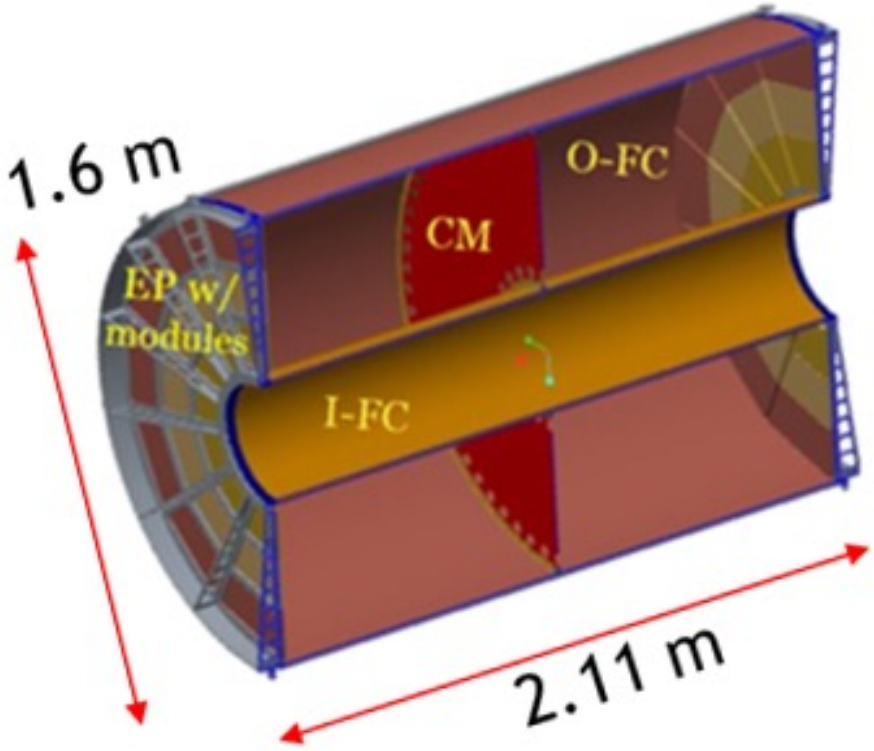
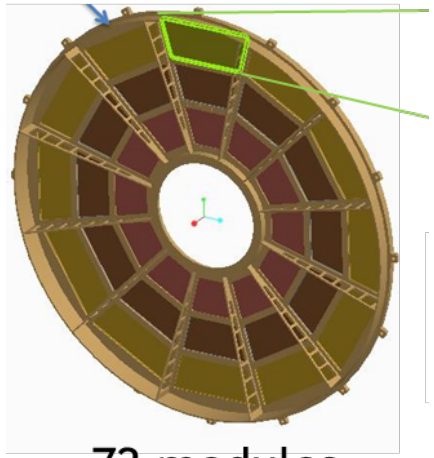
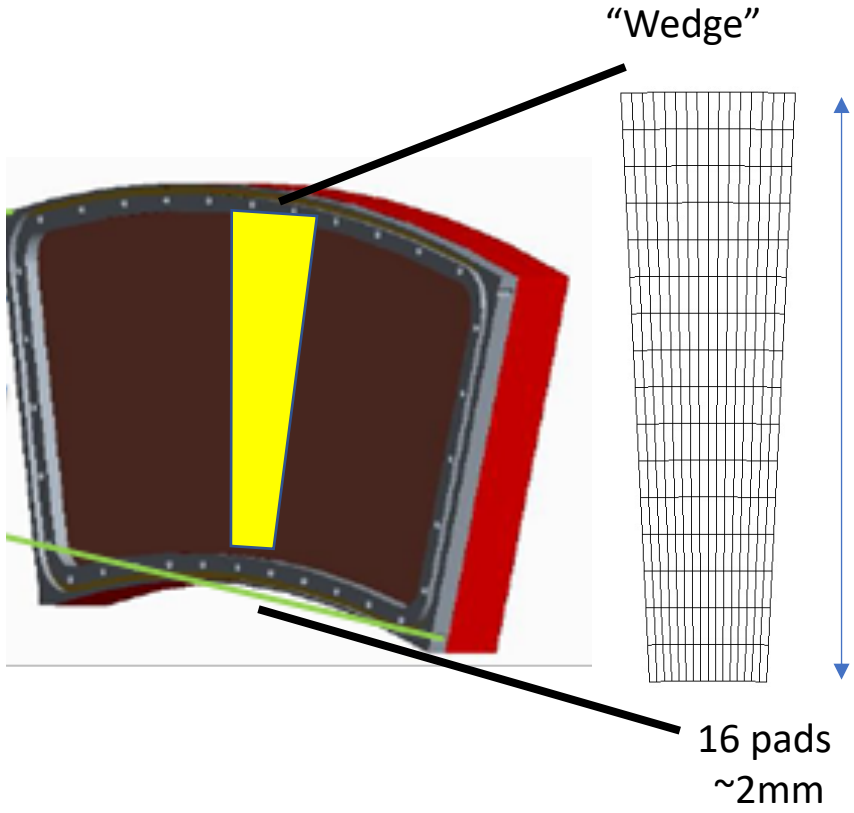
sPHENIX TPC

- Primary device for tracking and momentum measurement
- Fiducial volume: 20<r<80cm, full azimuth, $|\eta|<1.1$ (@r=80cm)
- Event rate: ~15-100kHz (sqrt(s_{NN})=200GeV, Au+Au collisions)
- Goal is to achieve 100-150μm position resolution in the fiducial volume



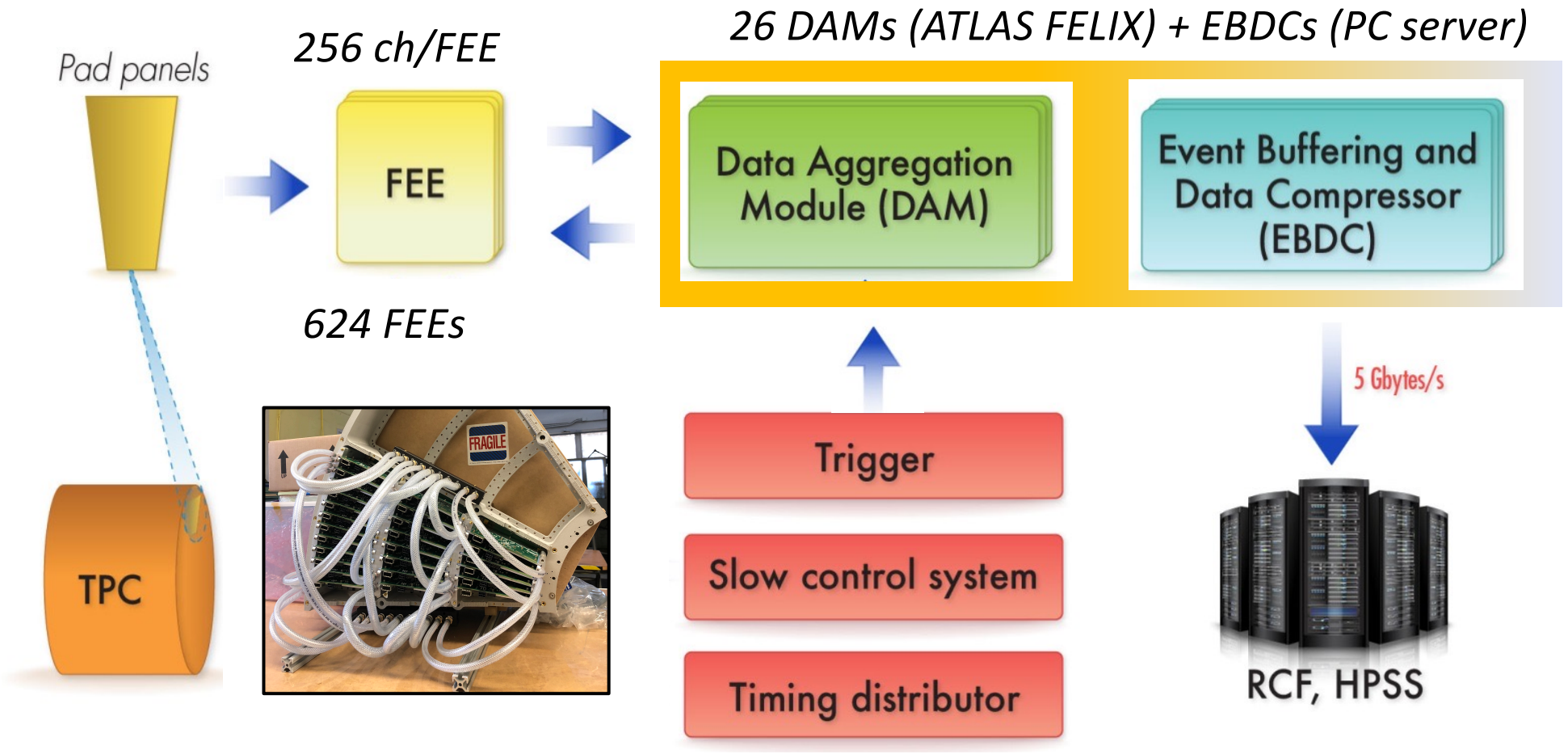


72 modules
2(z), 12(ϕ), 3(r)



sPHENIX TPC readout system

- Overall readout scheme: padplane -> FEE -> DAM+EBDC -> Storage
- Data rate: ~10Mbits per Au+Au MB events from whole TPC



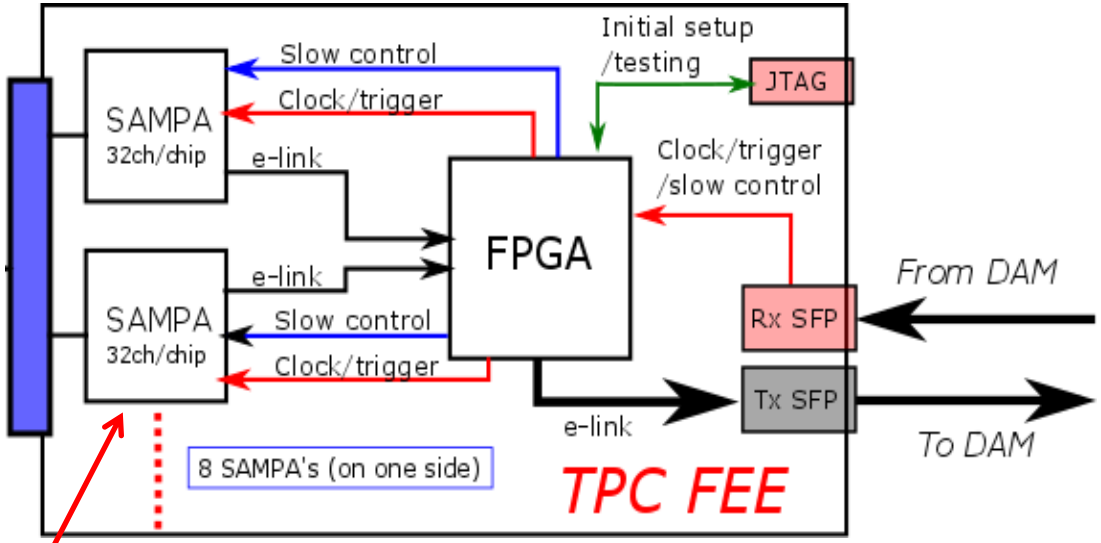
Total # of FEEs is 624

# of FEEs per sector:
- 6 for 20<r<40cm
- 8 for 40<r<60cm
- 12 for 60<r<78cm

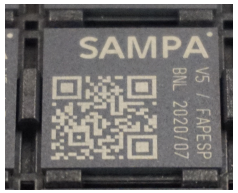
1 sector = 2π/12 per side

Front End Electronics (FEE)

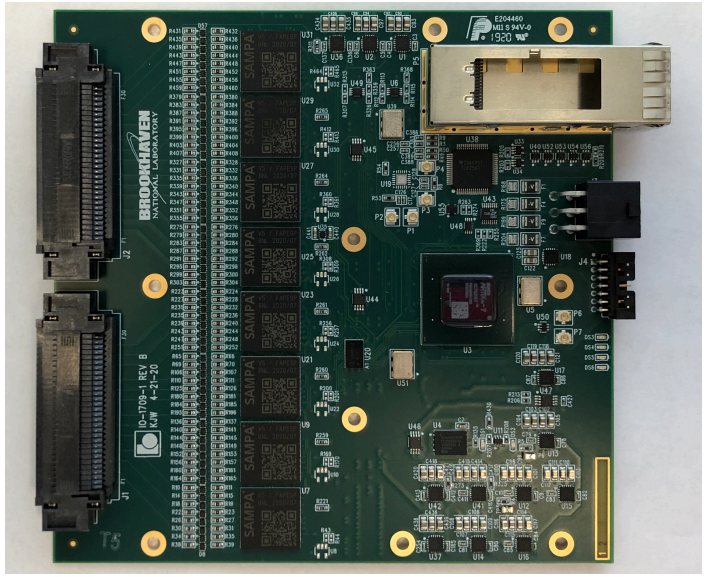
- **Continuous readout mode**
- Use of 8 SAMPA chips per FEE (256ch/FEE)
- Use of newly developed SAMPA v5 that has 80nsec shaping time option.
  - 160nsec is also available
- FPGA receives data from SAMPA and sends to optical link, and processes clock and slow control data from DAM.
  - JTAG is implemented over optical link.
  - Two data links are available
- ADC clock will be 4.7, 9.4 or 18.8 MHz, as we base on the RHIC beam-crossing clock.
- Power consumption: ~15W per card



SAMPA v5



Pre-production
FEE board



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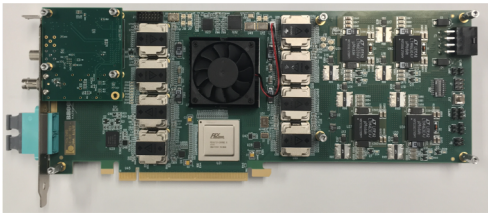
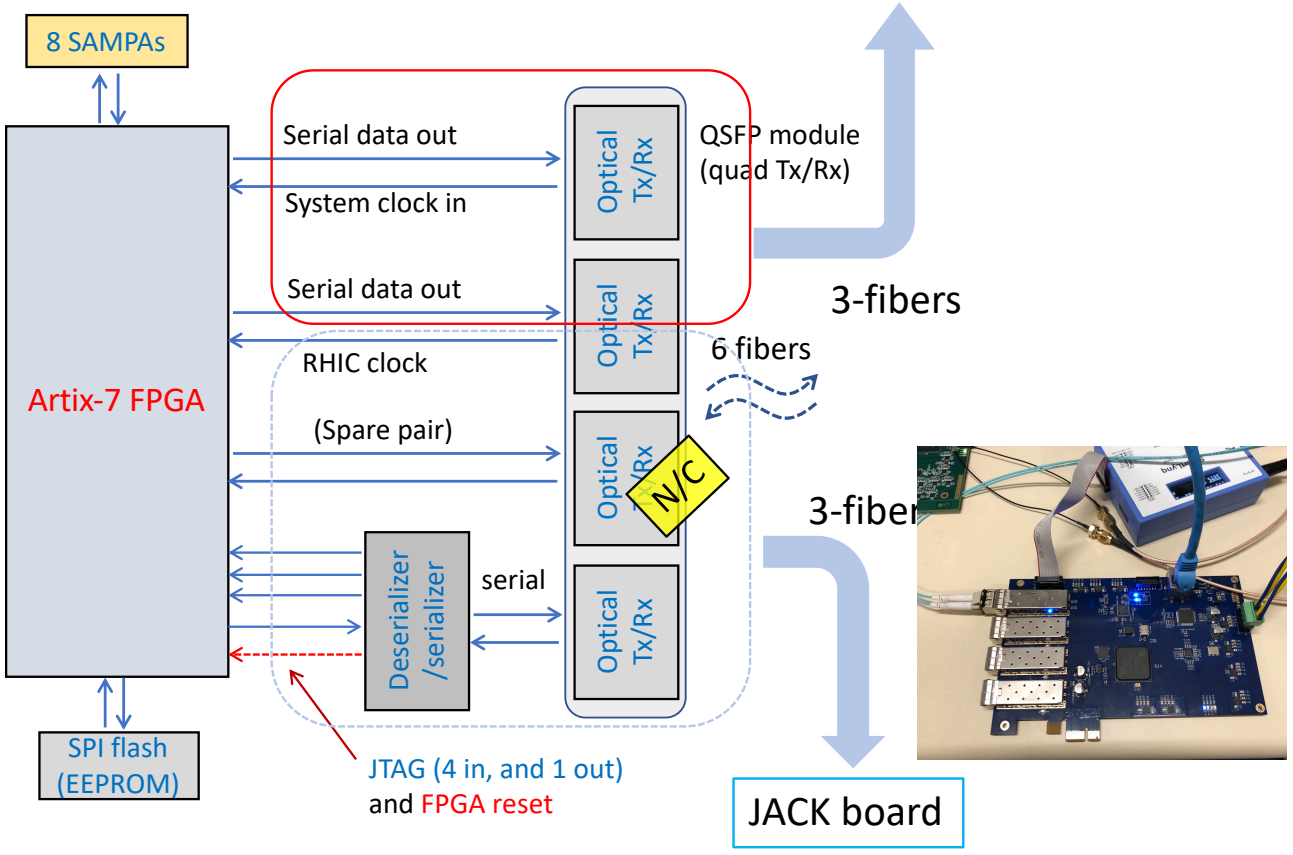


DAM board

FEE diagram around FPGA

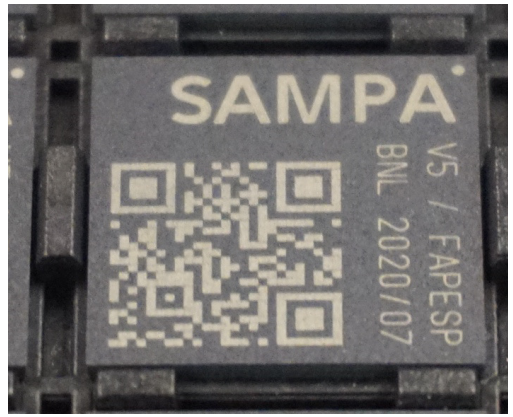


SAMPA chip feature (v4)

- SAMPA = 32 ch * (CSA + Shaper + FADC) + DSP
- CSA (pos/neg input) + Shaper: see table
- FADC (10bits) sampling: 5, 10, and 20MHz.
- DSP functions:
  - Data buffering and packeting (header etc.)
  - Three baseline correction (restoration) schemes
  - Data reduction schemes are simple zero-suppression (ZS), cluster-sum after ZS applied, and Huffman compression (Never used)
- Operation mode
  - Triggered and trigger-less (continuous) readout mode
  - Direct ADC serialization
- Output: 11 e-links per chip.
  - 320Mbps per line → 3.2Gbps per chip
  - 10MHz sampling without zero-suppression is possible
- Good literatures:
  - https://readthedocs.web.cern.ch/ate/files/119245990/148606571/2/1592314724000/Sampa_V4_DataSheet.pdf
  - ALICE paper: https://doi.org/10.1088/1748-0221/16/03/P03022

Gain	Shaping time
30 mV/fC	160 ns
20 mV/fC	160 ns
4 mV/fC	300 ns

Power: ~1W per chip



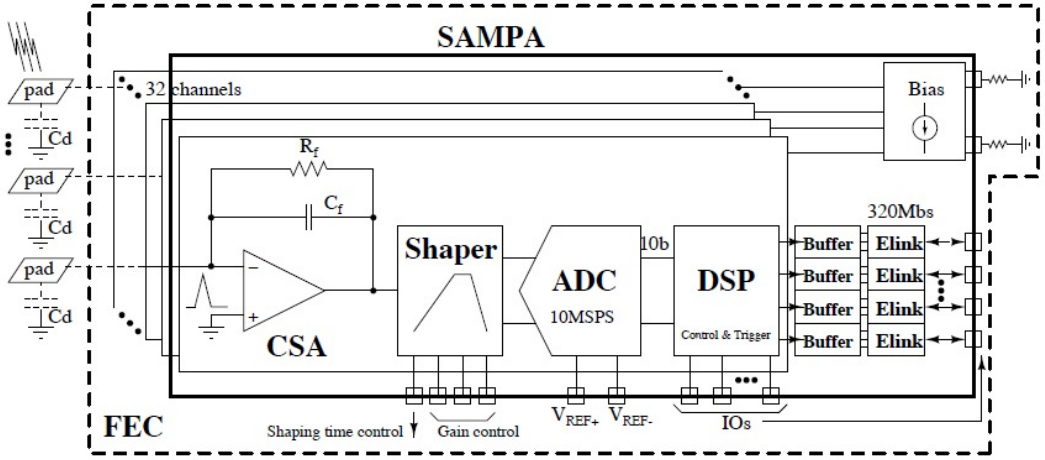


Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

SAMPA overall history

- MPW1 (multi-project wafer) is SAMPA “components”
  - 80, 160 and 300nsec shaping times were tested.
- MPW2 was the first integrated SAMPA chip
  - 80nsec was already dropped here.
- MWP3 (or SAMPA v3) was supposed to the ”production version”…
  - DSP issue was fixed, and pedestal memory part was redesigned to mitigate radiation issue.
  - Submitted for fabrication in early July 2017.
- MWP4 (or SAMPA v4) has shorter decay time for CSA (by changing R_f) for avoiding saturation by pile-up
  - Submitted for fabrication in early July 2017
- SAMPA v5 development for sPHENIX TPC from Apr 2018
  - Due to high hit occupancy in sPHENIX (Au+Au, 100KHz), shaping time faster than 160nsec was desired.
  - 80nsec shaping time is revived, in place of 300nsec
  - Modified FADC SAR switch for better ENOB

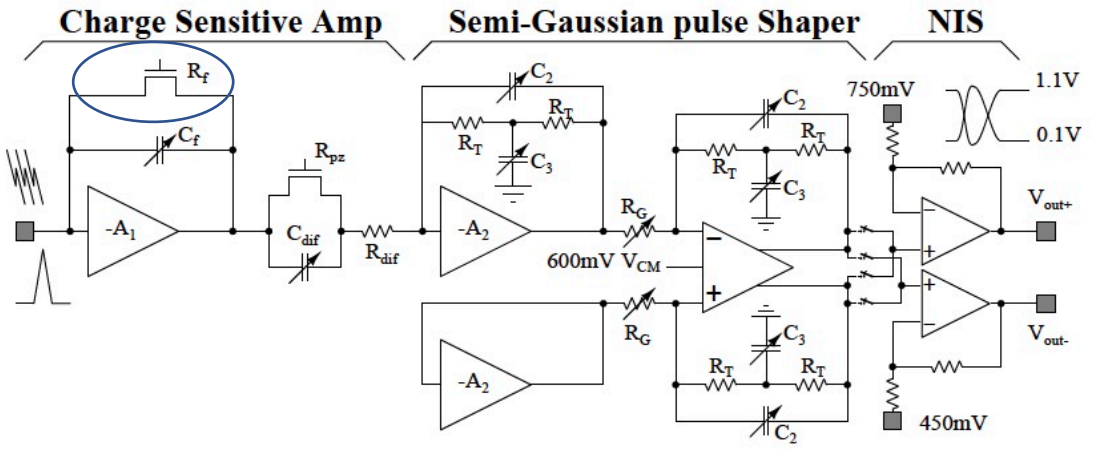
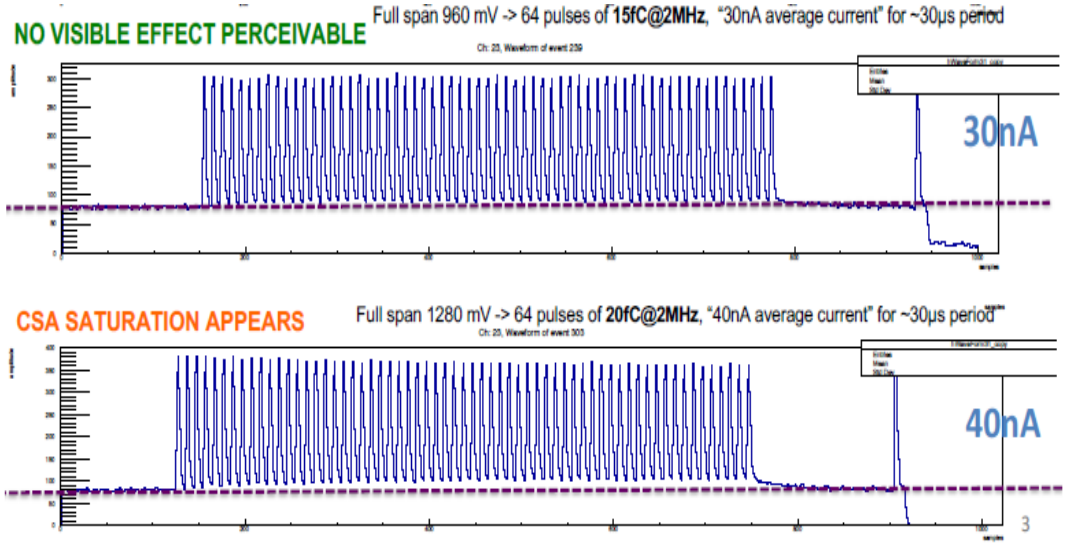


Figure 1.1: *Block diagram of the analog front-end.*



SAMPA v5 development history

- Simulation study started at U. Sao Paulo (USP) in Apr 2018
  - 80nsec shaping time revisited
- SAR ADC switching was also revised
  - Not implemented in v4 since the ENOB of ADC was already good for ALICE at that time.
  - Essential for 20MHz operation
- MPW design was submitted to TSMC in Oct, 2018
- MPW arrived at USP in Mar, 2019
  - Test was conducted by USP: Apr-Jun, 2019
  - At same time, the design of integrated chip (SAMPA v5) was performed.
- Full-chip production started Oct, 2019
  - First 4 wafers were delivered to USP and Lund in early Mar 2020 for initial testing.

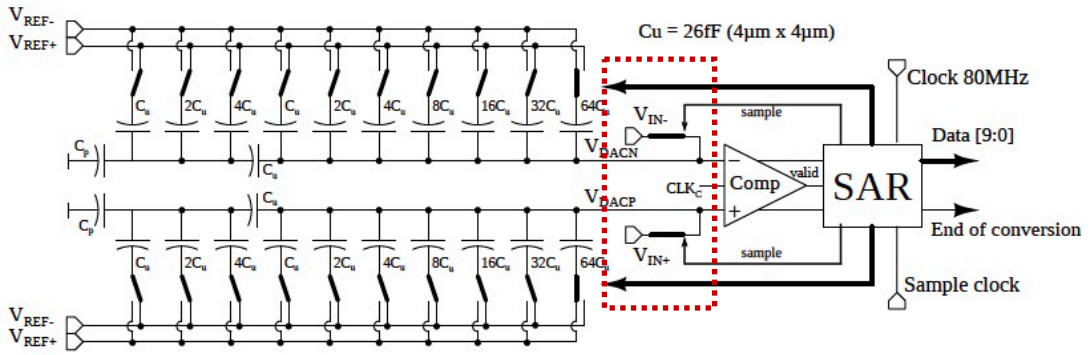
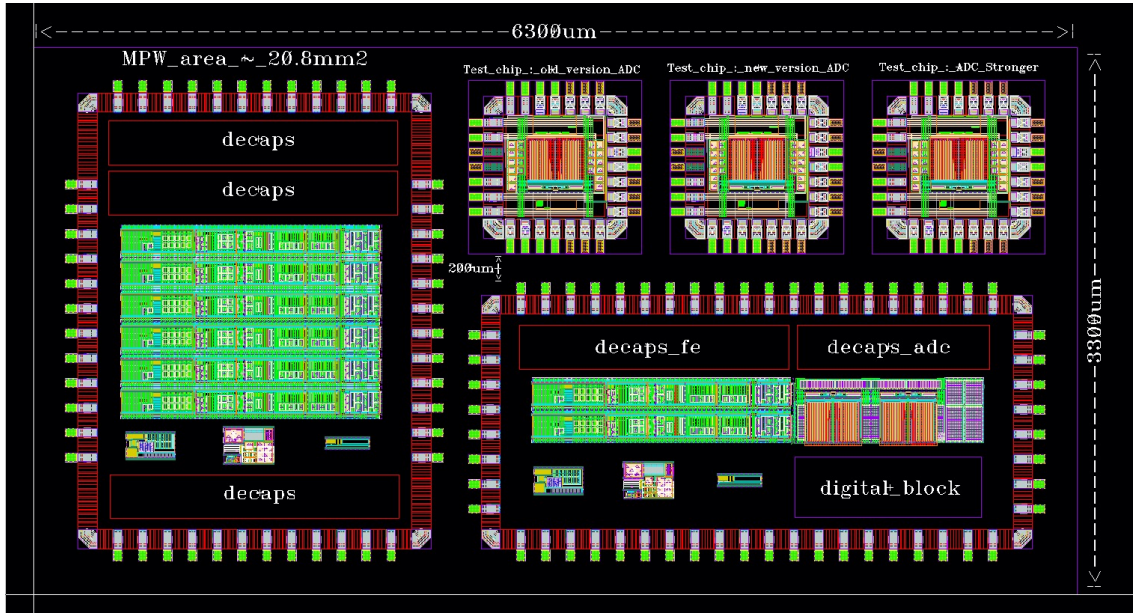


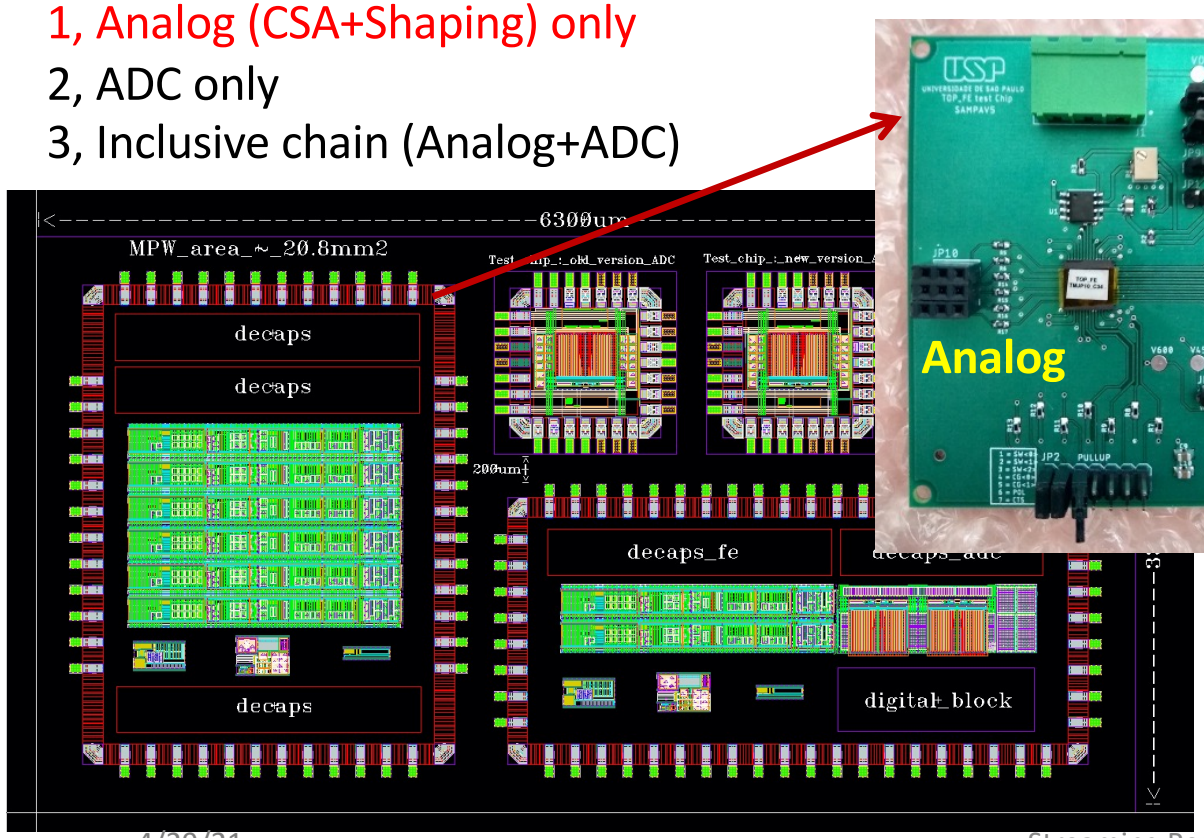
Figure 1.2: *Block diagram of the ADC.*

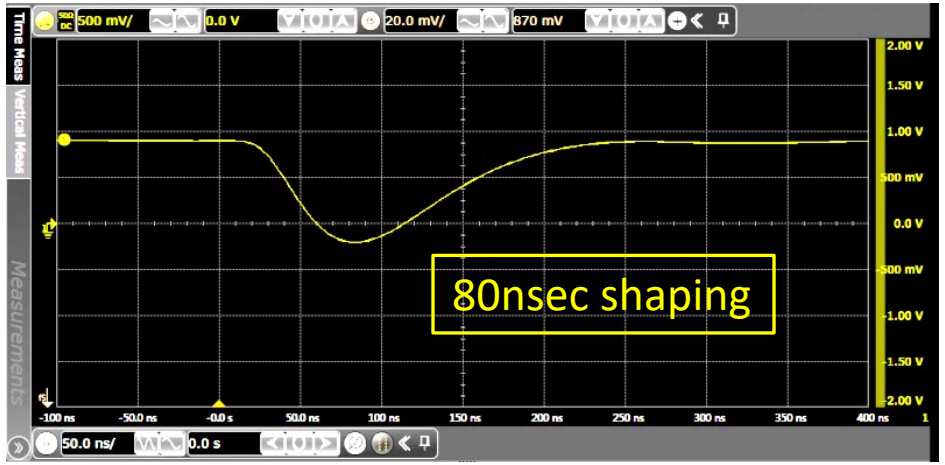


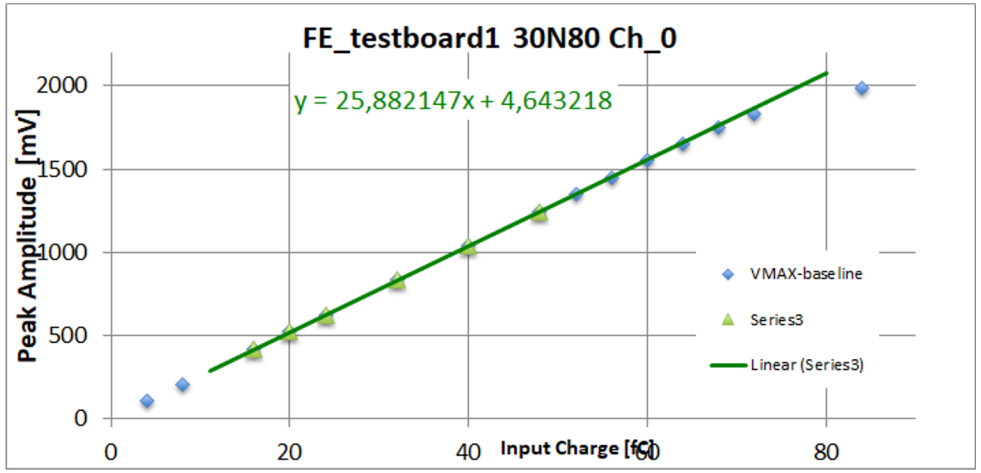
Test results from MPW chips (Analog)

- SAMPA v5 components were produced in a multi-project wafer (MPW) run
- Initial test shows a good linearity for 80nsec shaping and 30mV/fC gain.
  - Power consumption: 6mW/ch
  - Noise: ~500e @ C_{in}=0, ~600e @ C_{in}=20pF

1, Analog (CSA+Shaping) only
2, ADC only
3, Inclusive chain (Analog+ADC)





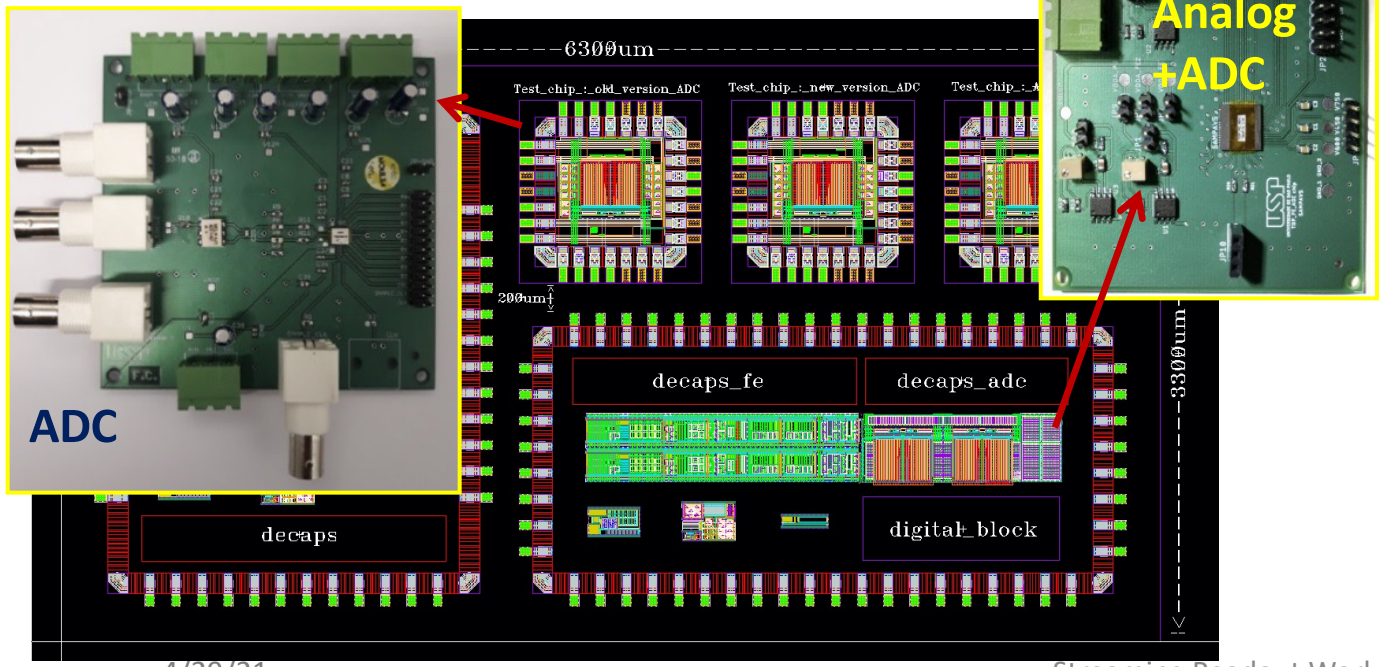


Test results from MPW chips (ADC)

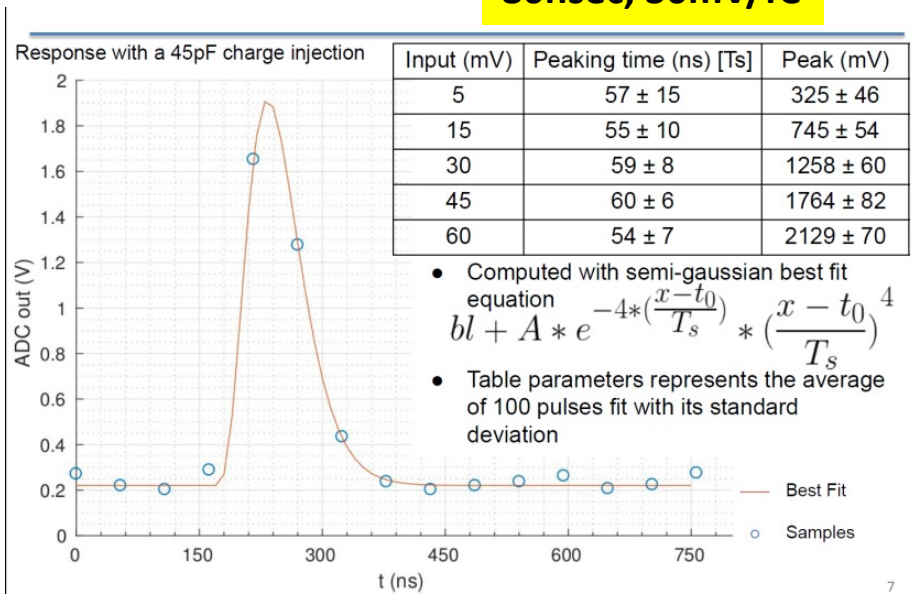
- ADC and Analog+ADC components
- ENOB of ADC is found to be better than that of SAMPA v4
  - Improvement at 18MHz is seen and is close to expected
- Pulse shape is successfully measured by Analog+ADC

1, Analog (CSA+Shaping) only
2, ADC only
3, Inclusive chain (Analog+ADC)

	18.5 MSPs	
Amplitude (% of maximum)	ADC V4 ENOB (bits)	ADC V5 ENOB avg. (bits)
40	9.2	9.2
50	8.6	9.1
70	8.6	8.9
90	8.2	8.7



80nsec, 30mV/fC

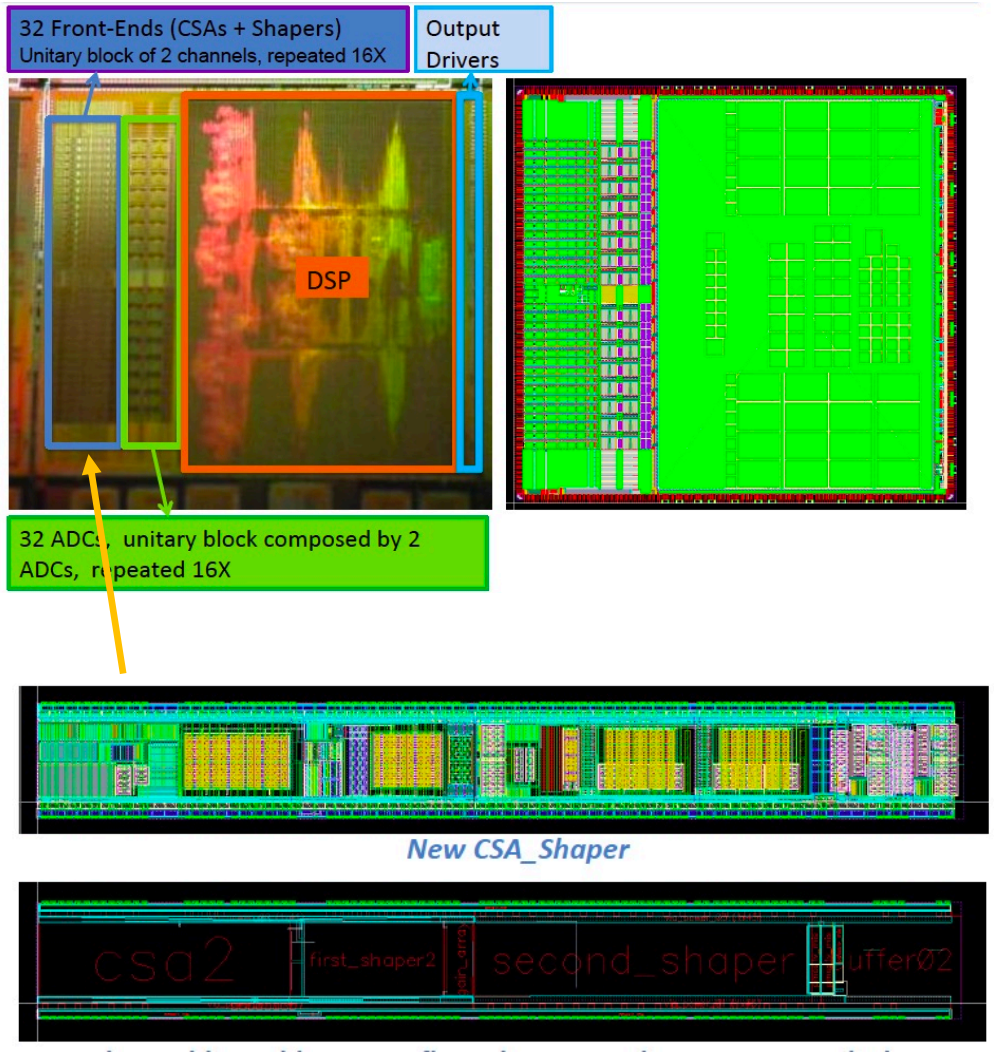


Input (mV)	Peaking time (ns) [Ts]	Peak (mV)
5	57 ± 15	325 ± 46
15	55 ± 10	745 ± 54
30	59 ± 8	1258 ± 60
45	60 ± 6	1764 ± 82
60	54 ± 7	2129 ± 70

- Computed with semi-gaussian best fit equation $bl + A * e^{-4*(\frac{x-t_0}{T_s})} * (\frac{x-t_0}{T_s})^4$
- Table parameters represents the average of 100 pulses fit with its standard deviation

Production of SAMPA v5 chips

- New CSA, Shaper, and FADC circuits were integrated to the “SAMPA” chip
  - Layout were rechecked
- Produced wafers from so-called MLM maskset
- Total chips produced: ~12k
  - # of chips absolutely needed is 4992.
  - Chips per wafer is ~264
  - An engineering run produced 21 wafers: ~5500 chips
  - A production run gives 25 wafers: ~6600 chip
- Production history
  - Processed first 4 of 21 wafers to the final packaged chips (~1000 chips)
  - Rest 17 of 21 wafers were held at contact level
  - Proceed to packaging for the 17 wafers and run another 25 wafers after the 1000 chips were confirmed fine
- If you are interested in cost, ask offline.



Test results from production chips

- Detail test results from U. Sao Paulo
- Noise look somewhat larger than expected, due to noise from the test board
- Very good linearity was observed
- Peaking time is shorter than defined

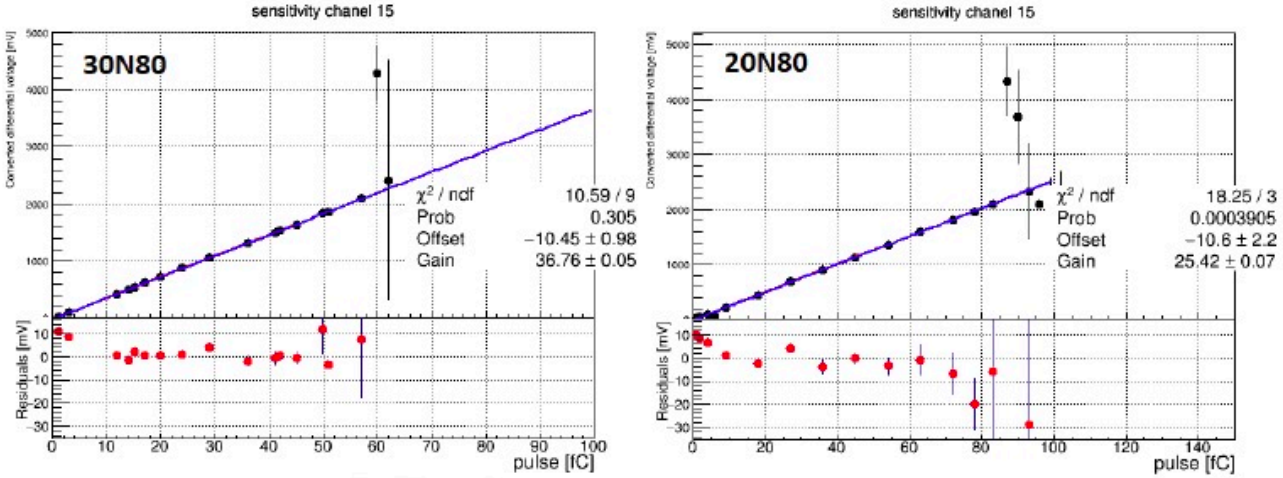
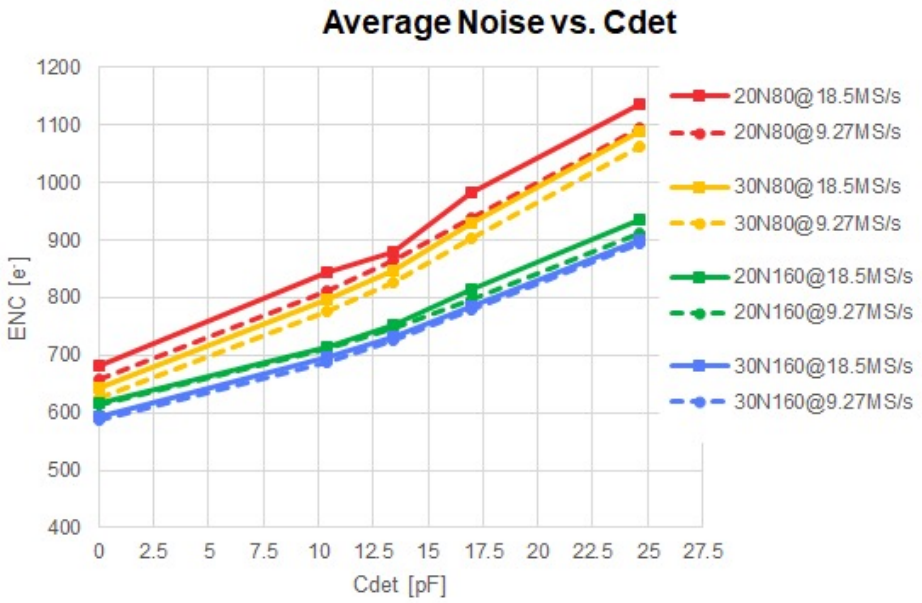
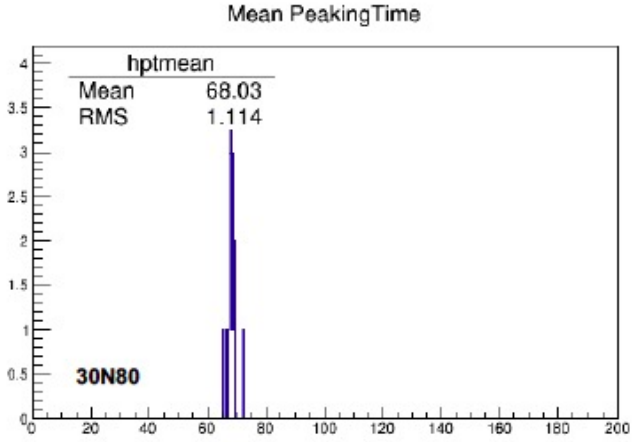
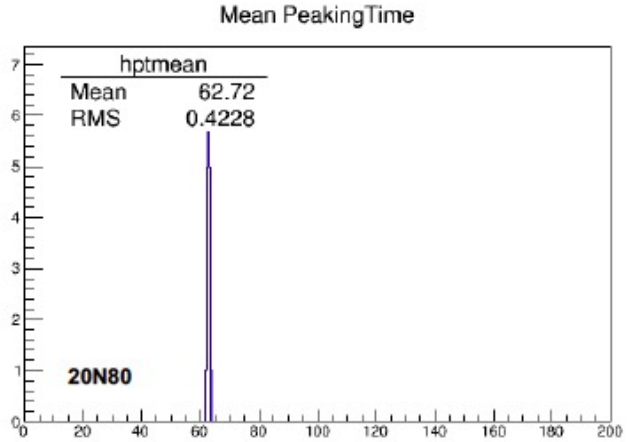


Figure 10.1: Sensitivity for one channel of sample 11 at 18.542 MS/s.



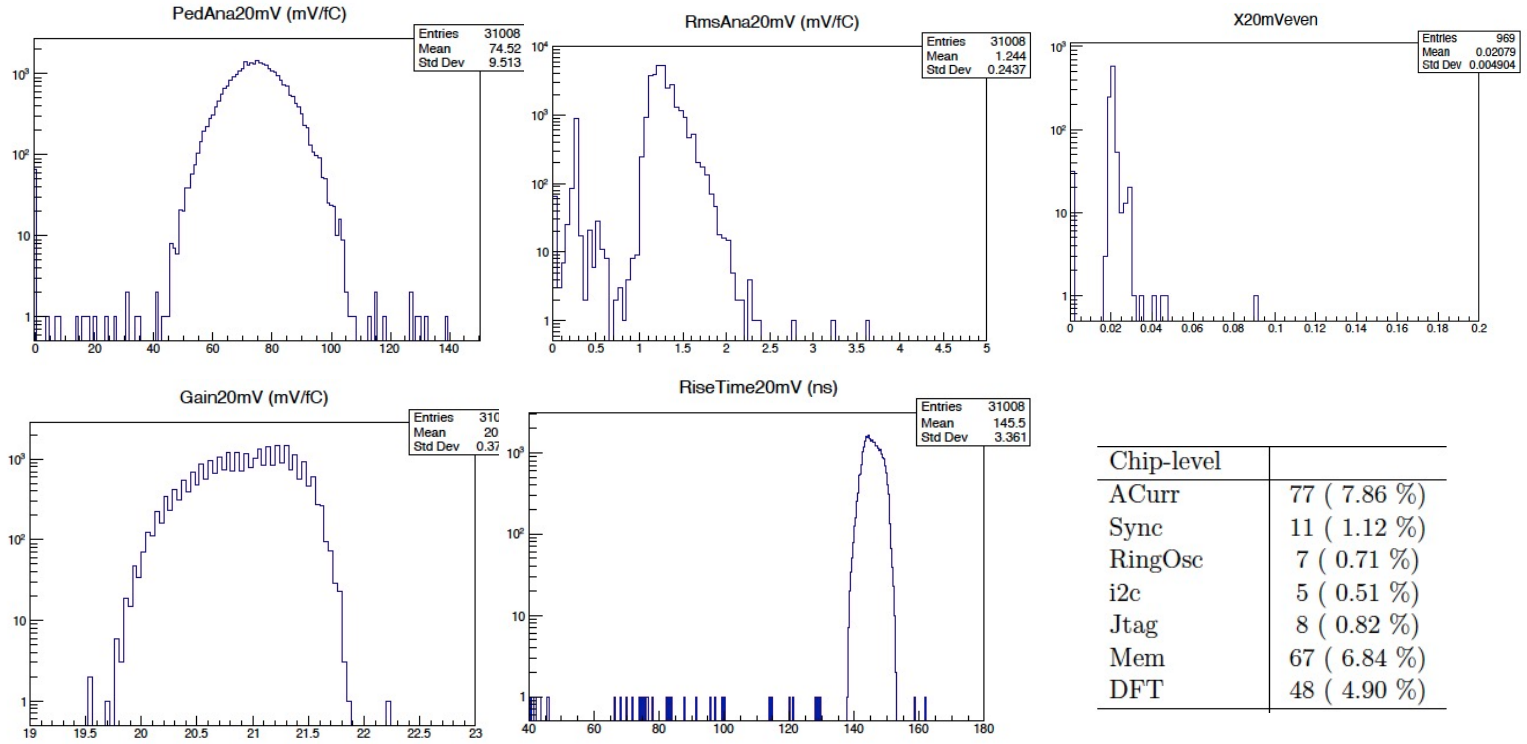




Mass chip testing at Lund University

- Robot testing stand was built at Lund University (Sweden) for ALICE. Lund joined sPHENIX lately
- Two pass testing: 160nsec and 80nsec. Same testing items as for ALICE TPC/MuCH
- SAMPA v5 test at 160nsec is finished. Yield is ~70%. 80nsec test in progress

https://youtu.be/3tnqPbMWzqQ

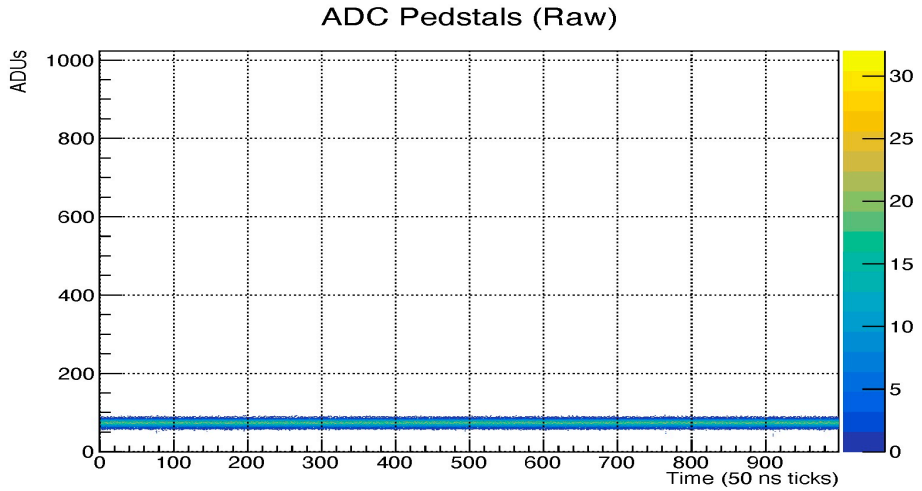


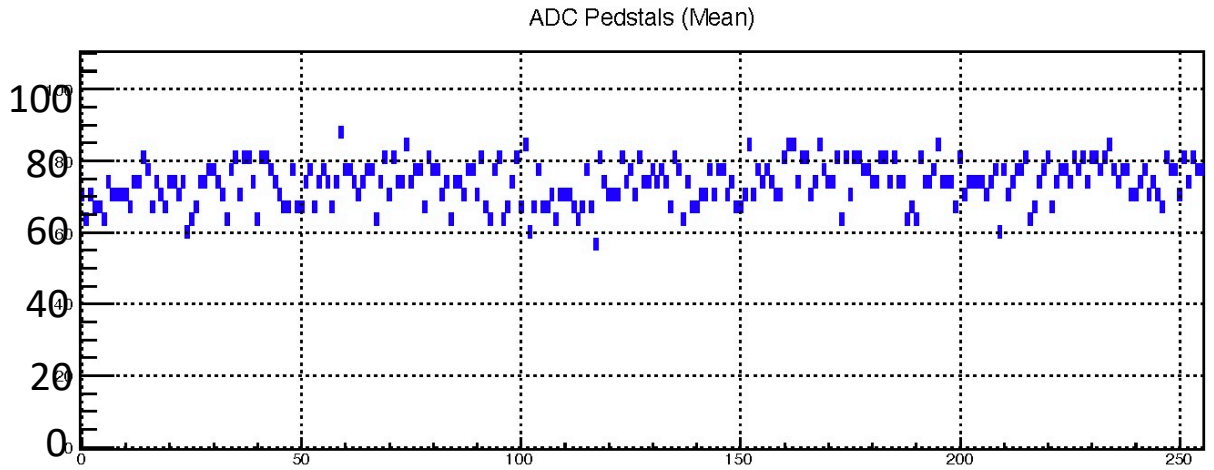
Chip-level	
ACurr	77 (7.86 %)
Sync	11 (1.12 %)
RingOsc	7 (0.71 %)
i2c	5 (0.51 %)
Jtag	8 (0.82 %)
Mem	67 (6.84 %)
DFT	48 (4.90 %)

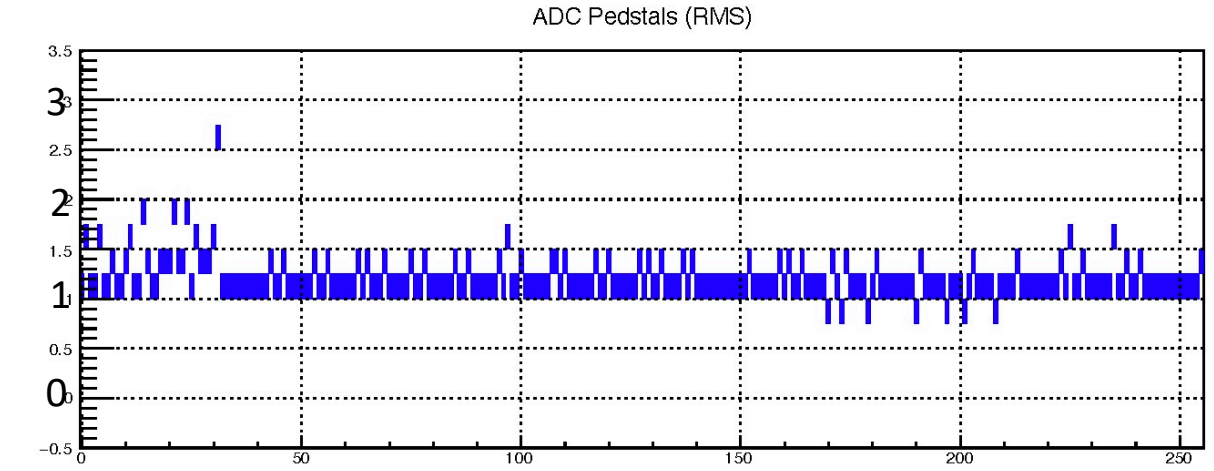
Testing results at 160nsec shaping from the first 980 chips

SAMPA data from Pre-production FEE

- Pedestals of 256 channel output from the pre-production version of FEE cards
- No detector or capacitance to input (C_{det}=0)
- 80nsec shaping, 20mV/fC, 20MHz sampling
- No zero-suppression, no base-line correction
- RMS of ~1.2 ADU corresponding to ~700 e







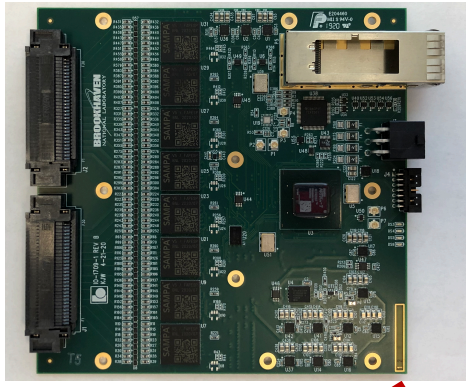
channels

Plots made by John Kuczewski (IO)

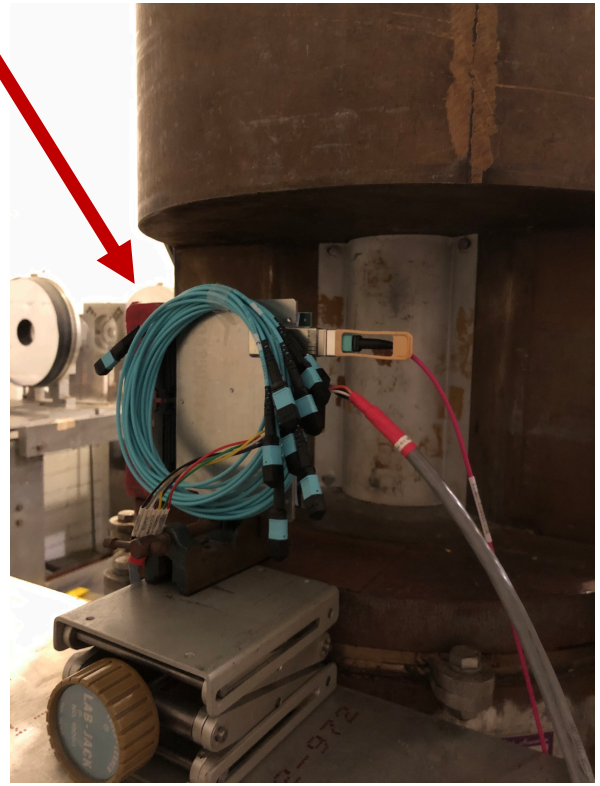
Radiation hardness test

- Radiation hardness requirement for FEE
  - 25krad TID for 5 yrs. We require 100krad hardness.

- Test at ^{60}Co γ source (10krad/hr) at BNL
  - Most of the parts passed the test. Failed parts were replaced with alternate parts later.
  - SAMPA was turned on and data are readout normally. Pedestals are fine. (130nm CMOS is good)



We also performed magnet field test (1.5T), but saw no effect to components (incl optical Tx/Rx)



Manufacturer	Part Number	Description	Test date	Result
TSMC and USP	SAMPA ver4	CSA + Shaper + ADC + DSP	8/2/2019	OK up to 100krad
TI	TPS7A8500RGRT	IC REG LINEAR POS ADJ 4A 20VQFN	7/18/2018	OK up to 100krad
ON Semi	CAT102TDI-GT3	IC VREF SHUNT ADJ TSOT23-5	12/10/2018	dead at 50krad
ON Semi	NUP4114UPXV6T1G	TVS DIODE 5.5VWM 10VC SOT563	8/2/2019	OK up to 100krad
TI	PCA9306DCUR	IC VOLT LEVEL TRANSLATOR US8	8/2/2019	OK up to 100krad
TI	SN74AVC16T245ZQLR	IC BUS TRANSCVR 16BIT 56BGA	8/2/2019	OK up to 100krad
TI	SN74LVC2G04DCKR	IC DUAL INVERTER GATE SC-70-6	8/2/2019	OK up to 100krad
Linear	LTC2991CMS#PBF	IC MONITOR OCTAL 16-MSOP	N/A	
Macronix	MX25L25735FZ2I-10G	IC FLASH 256MBIT 104MHZ 8WSON	12/10/2018	OK at 20krad, dead at 50krad
Abracon	ASDMB-50.000MHZ-LC-T	OSC MEMS 50.000MHZ CMOS SMD	8/2/2019	OK up to 100krad
Maxim	DS620U+	SENSOR TEMPERATURE I2C 8UMAX	N/A	
Many	EG-2101CA	OSC XO TBD MHZ LVDS 6-SMD, NO LEAD	8/2/2019	OK up to 100krad
Silicon Labs	SI5338B-B-GMR	IC CLK GEN I2C QUAD 24QFN	8/2/2019	OK up to 50krad, dead at 80krad
AVAGO	AFBR-57D7APZ	850nm optical Rx/Tx	7/18/2018	OK up to 100krad

Summary, TODO, and future

- SAMPA v5 development has been successfully completed
  - ~12k chips have been produced which are more than what sPHENIX TPC FEE will need
  - So far, performance meets our expectation.

- More detailed test of the SAMPA on FEE as well as system integration test are on-going
  - Saturation characteristics (baseline shift)
  - Spark protection test, and several other stress test

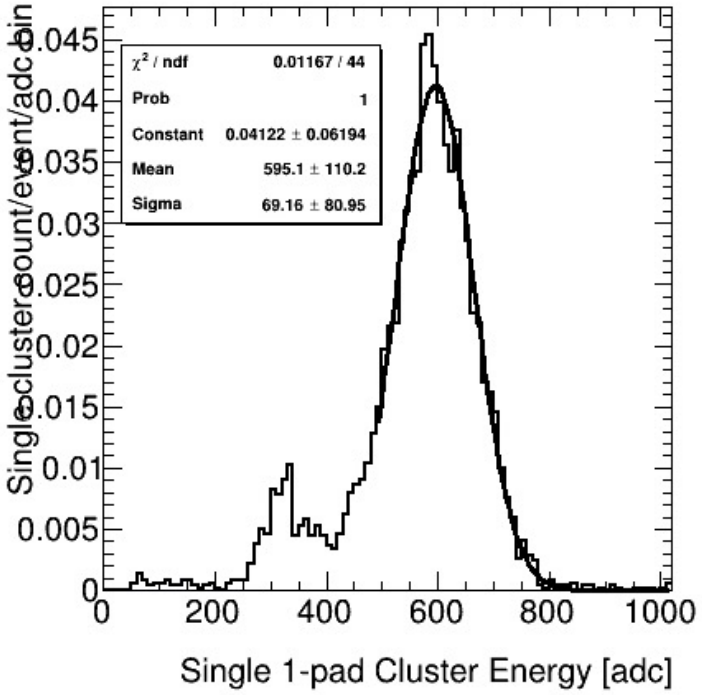
- Implementing SEU mitigation for the FEE, mainly for the FPGA
  - SEU for the SAMPA is not critical for operation. It should be less frequent than FPGA.
  - If happens, SAMPA will be reset by FPGA.

- Future of SAMPA
  - TSMC decided to finish producing wafers from MLM masks and the last order with a month ago
    - Some interested parties negotiated with the company at that time.
  - Additional SAMPA chips can still be made but will need to make a new ”full” maskset
    - Making full maskset is straightforward. A software can produce it from the existing design file.
    - Cost for the full maskset production is about twice as expensive as MLM maskset.

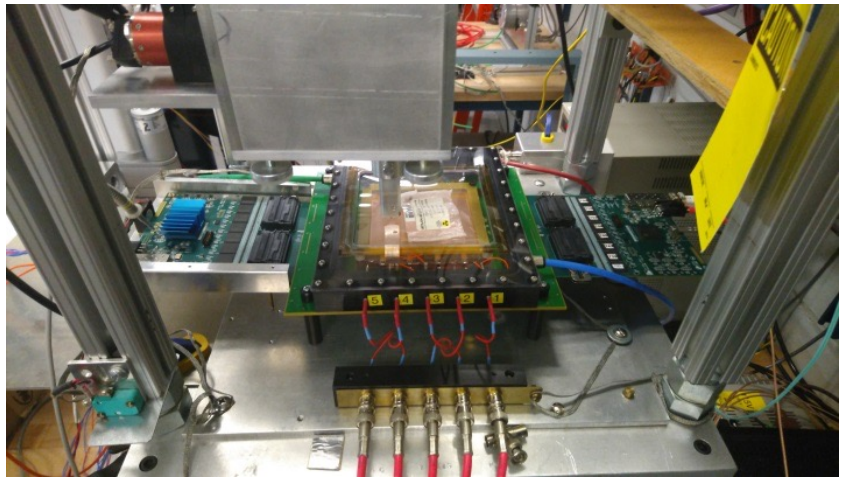
Backup

FEE prototype around v2 and v4 chips

- Signal from X-ray gun (X-ray fluorescence on ^{55}Mn) to a GEM chamber at has been readout by the prototype FEE (256 channels)



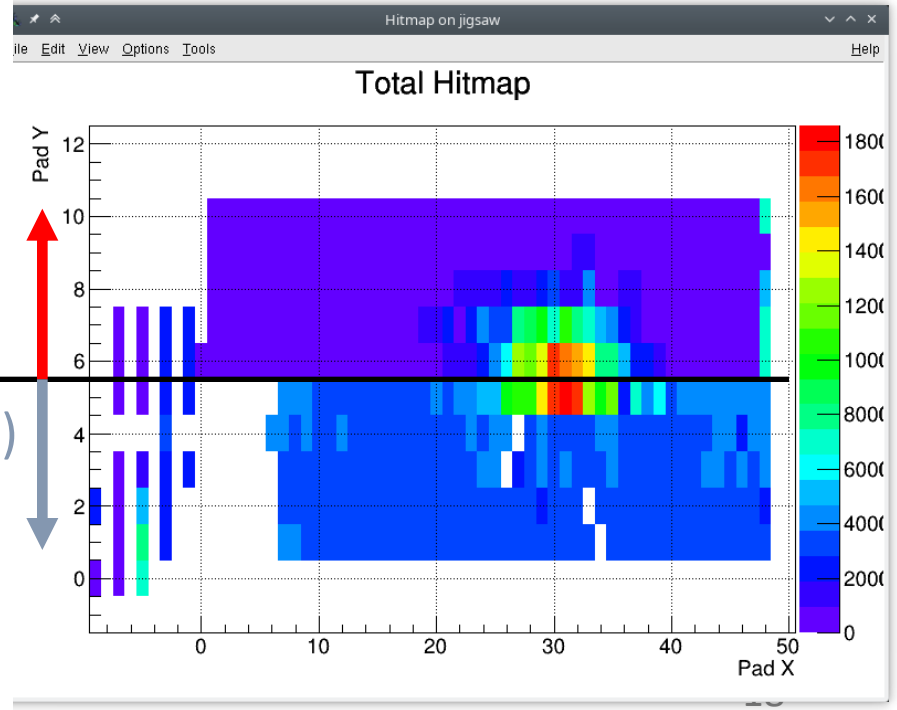
- Hit distribution from ^{55}Fe over two FEEs
  - **Proof-of-principle that DAM properly handles data from multiple-FEEs**
  - **Data taken by John Kuczewski**



Plot made by Jin

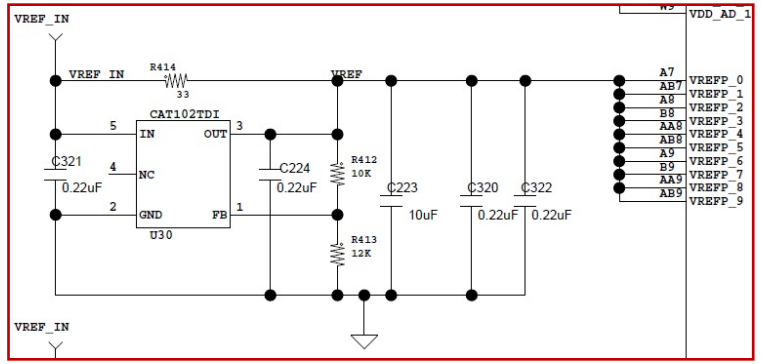
Up: FEE1 (SAMPA v4)

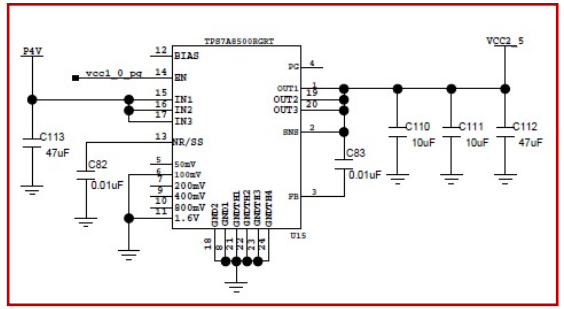
Down: FEE0 (SAMPA v2)



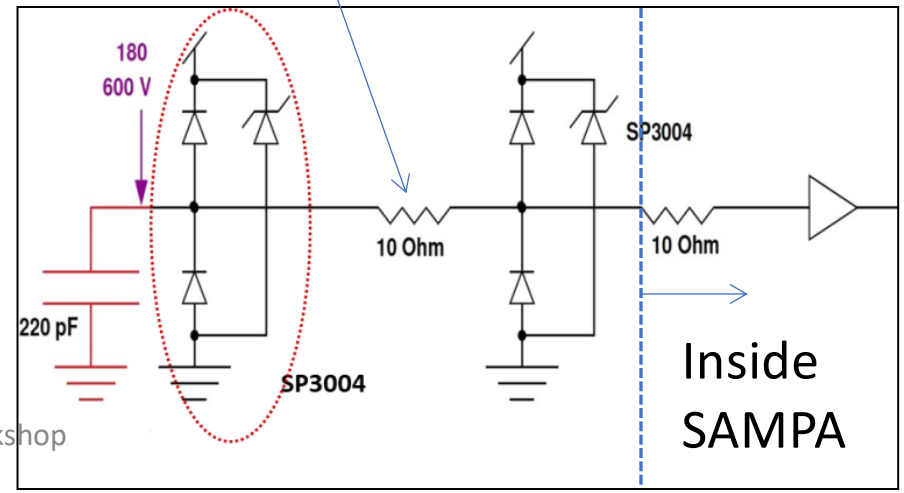
Revision for pre-production board

- ADC reference regulator was replaced
  - CAT102 (one for each SAMPA) with the one used for power regulation (TI TPS7A8500RGRT)
  - One TPS7A8500RGRT takes care of 4 SAMPAs.
    - Decoupling cap will be placed near each SAMPA.
- PLL bypass pads were added for keeping option of removing it at a later time
- New spark protection is implemented.
  - Resistor size is increased from 0201 to 0603.
  - Even ALICE's resistors can be used.
- Largest FPGA, Artix-7 200T (was 100T)
- New SPI flash (EEPROM) for FPGA
  - Cypress S25FL256SAGMFIR01
  - ATLAS confirmed it works upto 40krad





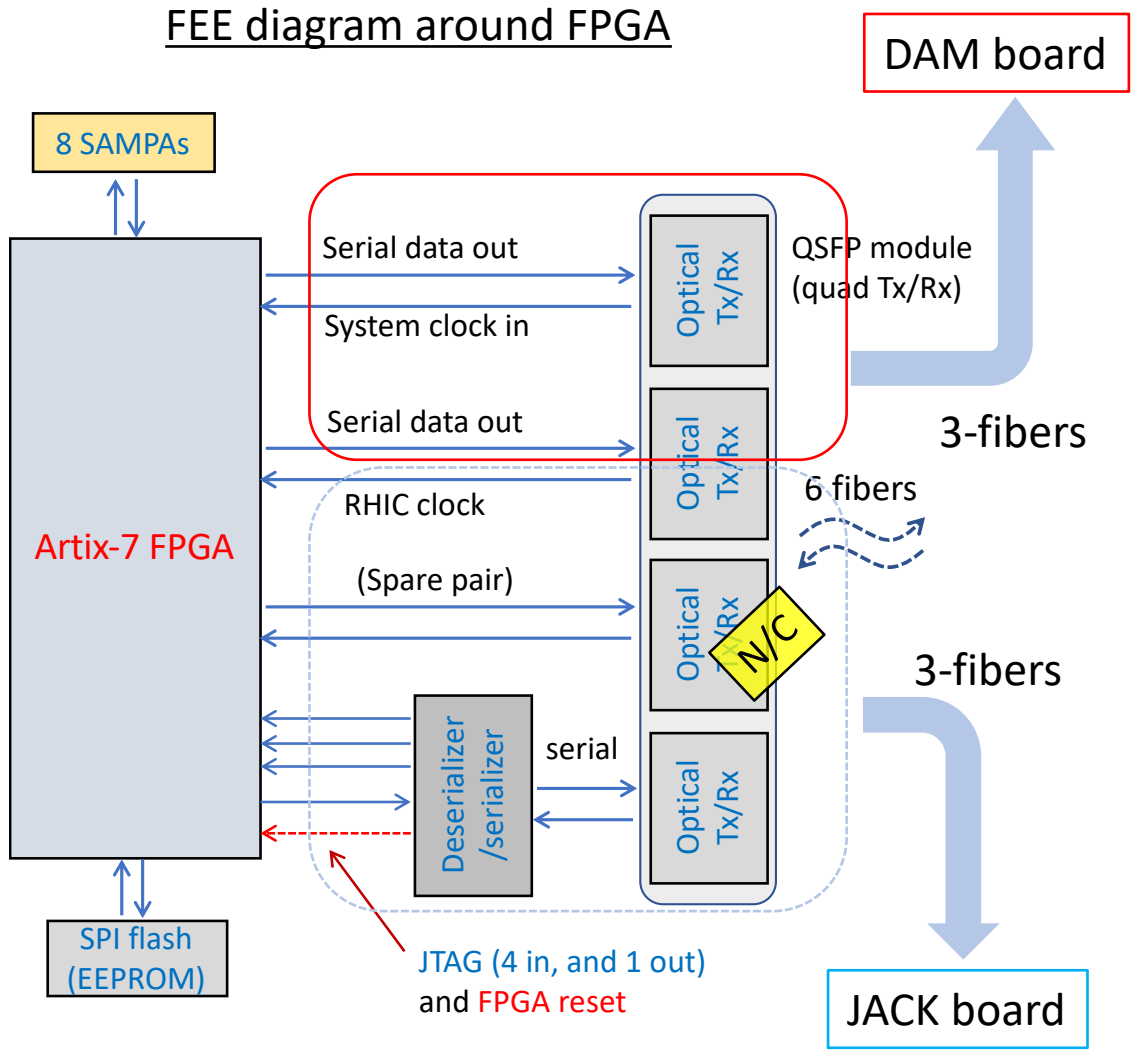
ROHM KTR03EZPF1000
(0603)



JACK development

- Clock:
  - RHIC clock has been recovered through slow-control fiber line now.
  - A dedicated clock line will make the clock synchronizing scheme simpler

- JTAG (over optical fiber):
  - JTAG was primarily for programming FPGA on FEE, in case EEPROM was dead by radiation
  - It turned out that the JTAG connection is very useful for mitigating single event upset (SEU) of the FPGA.
  - FPGA reset without power recycle is implemented only through JTAG



Single event effect on FPGA

- Xilinx Artix-7 7A200T FPGA
- Assuming all CRAM bits are significant
- Used AMPT event generator (Au+Au 200GeV @100KHz) to estimate charged hardron rate at particular positions.
- Triple modular redundancy (TMR), memory scrubbing is implemented

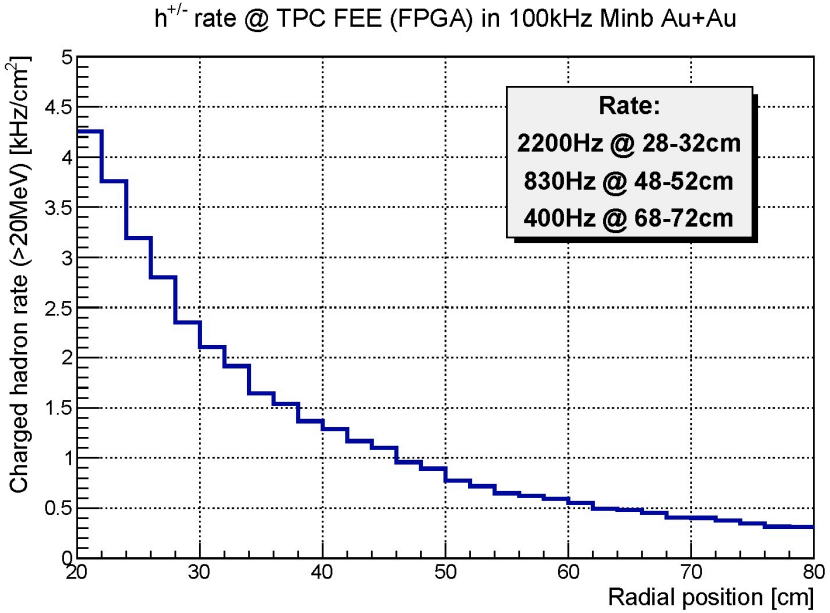
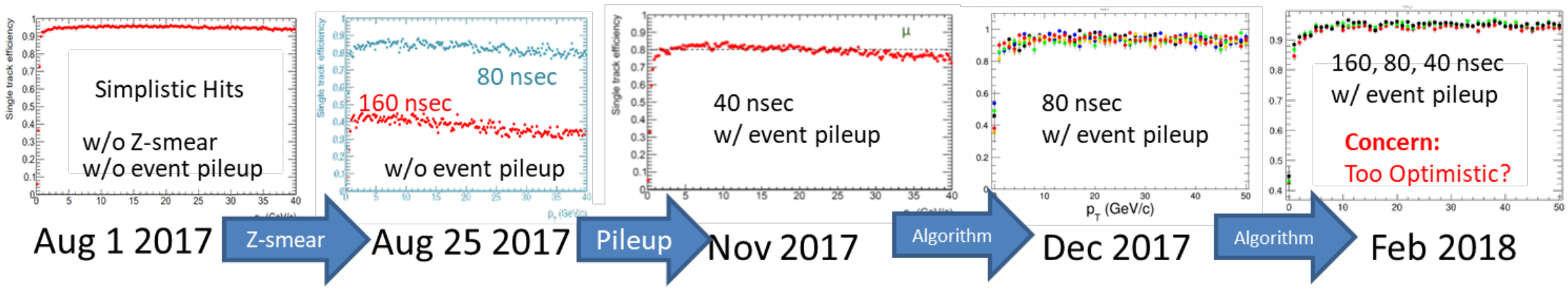


Table 2.7: Soft error for sPHENIX TPC FEE case (using Artix-7 7A200T).

R-position	# of FEE	flux [Hz/cm^2]	error/FEE [s^{-1}]	error/sector [s^{-1}]
28-32cm	120	2200	1.6×10^{-6}	1.9×10^{-4}
48-52cm	192	800	5.8×10^{-7}	1.1×10^{-4}
68-72cm	288	400	2.9×10^{-7}	8.6×10^{-5}

One error in 45 minutes as whole TPC

25kRad TID for 5 years.
1.2 10^{12} 1MeV-eq n/cm^2


Simplistic Hits
w/o Z-smear
w/o event pileup
80 nsec
160 nsec
w/o event pileup
40 nsec
w/ event pileup
80 nsec
w/ event pileup
160, 80, 40 nsec
w/ event pileup
Concern:
Too Optimistic?
Aug 1 2017
Z-smear
Aug 25 2017
Pileup
Nov 2017
Algorithm
Dec 2017
Algorithm
Feb 2018