

ROBUST HIGH-PERFORMANCE MICROELECTRONICS

Update on Alphacore's Readout ICs

Streaming Readout Workshop VII April 29, 2021



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Outline

- Alphacore's 90nm 180nm CMOS preamplifiers and ADCs status
- Alphacore's 22nm 28nm CMOS ADCs status



Alphacore's Goals

- Alphacore has been a performer in a DOE STTR Ph2 program entitled: "Multi-Channel Readout IC for Nuclear Physics Experiments" and in a DOE SBIR Ph2 program entitled: "Picosecond Digitizer".
- Status: The funded technical periods ended in May and August, respectively. Alphacore is wrapping up the programs and seeking further funding opportunities.
- Key goal of these programs has been to develop versatile detector readout solutions, both IP and ICs.
- The IP blocks can be used to relatively quickly build the exact, compact readout ASICs configurations most suitable for a target application when the need arises. Alphacore can build the exact ASIC for a customer in need using the tested IP.



Summary of Recent Readout Circuit Designs

	22nm – 28nm CMOS readout circuits	90nm - 180nm CMOS readout ckts	
Main funding source	DOE HEP SBIR Ph2 (until August 2020)	DOE NP STTR Ph2 (until May 2020)	
Silicon-Evaluated Design #1	28nm, 10b, 300MSPS, 0.8mW ADC	180nm programmable preamplifier	
Silicon-Evaluated Design #2	28nm 10b, 500MSPS, 1.2mW ADC	180nm 10b, 50MSPS, 7mW ADC (1-ch, 6-ch)	
Silicon-Evaluated Design #3	28nm, 9b, 1GSPS, 2mW ADC	180nm 12b, 100MSPS, 60mW ADC (1-ch, 6-ch)	
Silicon-Evaluated Design #4	28nm, 10b, 2.4GSPS, 6mW ADC	180nm serializer interface with PLL	
Silicon-Evaluated Design #5	22nm, 10b, 5GSPS, 19mW ADC	90nm 14b, 50MSPS, 35mW ADC	
Silicon-Deliverables now	Test boards for all ADCs (the output interface is not suitable for actual detector readout experiments)	Preamplifier and ADC single channel test boards, multichannel bare die	
Deliverables made available with small amount of additional funding	ADC chips and test boards with FIFO output interfaces suitable for detector readout experiments	Packaged multi-channel 180nm test chips	
Deliverables of potential follow-on program	Multichannel chips, FPGA based evaluation boards, improved specifications	Multi-channel 90nm chips, FPGA based evaluation boards, improved specifications, more channels per chip	



IP Library of 22nm and 28nm CMOS High-Performance Low-Power ADCs

- The library contains more than five 300MS/s 20GS/s ADCs.
- They are radiation tolerant designs and available for NP/HEP experiments.
- The ADCs can be delivered with "full raw data stream output interface" and/or with "digital waveform sampling buffer" FIFO output interface. The much simpler FIFO interface is enough for most nuclear physics experiments and it enables very low power dissipation and simpler board design.
- Next slides show examples of the library elements.



A10B500M: 10bit, 500MS/s, Ultra Low Power ADC



- Continuously sampling/ digitizing "no dead time" ADC
- Single channel ADC with wide input bandwidth (beyond 4th Nyquist zone)
- ENOB 8.0 8.9 over four Nyquist bands
- Ultra Low Power <1.18 mW (FOM <6.0fJ/conversion)



A9B1G: Wide Input BW, 9-bit, 1GS/s ADC



- Continuously sampling/digitizing "no dead time" ADC
- Single channel with wide input bandwidth (beyond 4th Nyquist zone)
- ENOB stays within 7.2-7.7 over the first four Nyquist bands
- Power <2.1mW (FOM = 10fJ/conv)
- Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GS/s

Output decimated by a factor of 91 in this test set-up



A10B2G: 10 bit, 2.4GS/s, Ultra Low Power ADC



- Continuously sampling/digitizing "no dead time" ADC.
- The ADC has an 8-way interleaved architecture, with combined sampling rate of 2.4GS/s. The sampling rate is limited by on-chip clock buffers. Optimized buffers would deliver up to 3.2GS/s with 6mW of additional power.
- We can interleave 16-way(on-chip) to achieve 6.4GS/s for continuous digitization with no dead time
- The developed calibration algorithm has been shown to be very effective for the calibration of interleaving spurs, in this case yielding SFDR of 60-70 dB and ENOB that varies from 7.9 bits to 8.5 bits in the first Nyquist band.
- Power = 6 mW (FOM = 6.9fJ/conv)





Ultra Low Power ADCs Walden Chart Comparison: FOM vs. Speed





Ultra Low Power ADCs Schreier FOM Comparison: FOM vs. Speed





180nm Charge Sensitive Amplifiers



Test chip for 3 CSAs

# specifications	CSA1 with programmability	CSA2	CSA3
Equivalent Noise Charge(ENC) worst case (electrons)	556	1.8K	480
ENC increase rate (electrons/pF)	22.25	negligible	22.25
Rise Time typical (ns)	92	208	20
Gain (mV/fC)	30.45	29.8	2.3
Rise time programmability (ns)	50n-200	NA	NA
Gain Programmability (mV/fC)	15-60	NA	NA
Fully Differential Output	Yes	Yes	Yes
Common Mode of Full Differential Output	0.8-1	0.8-1	0.8-1
Shaper Circuit	Yes	Yes	No



CSA Micrograph and Evaluation Boards

CSA evaluation boards and/or packaged chips are available for customers. 16-ch preamplifiers are available as bare die.





CSA measurement setup



CSA measurement test setup

Measured pulse waveforms on an oscilloscope Noise measurement with logic analyzer



CSA1 Test Results

Noise was measured as 430 electrons for 50pF detector capacitance



Shaping time programmability measurements



Gain programmability measurements



90nm – 180nm CMOS ADCs Test Results



ADC Test Setup



90nm, 14-bit, 50MS/s, 35mW ADC





180nm, 10-bit, 50MS/s, 7mW ADC Test Results



ADC test boards and/or packaged chips are available for customers. 6ch ADCs are available as bare die.

180nm Low-power High-Bandwidth I/O Interface Test Results







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180nm General Purpose PLL for Serializer, Test Results

Alphacore's PLL

- Output frequency range: 80 to 800 MHz
- Power at 1.8V supply: 3.69 mW





A performance summary of Alphacore's PLL

Input Freq. (MHz)	Output Freq. (MHz)	Lock time	Phase noise	RMS jitter (ps)	Peak-to-peak Jitter(ps)	
50	200	2.3us	-144.16 dBc/Hz @10MHz	0.339	2.09502	
75	300	1.5 us	-141.688 dBc/Hz @10MHz	0.304	1.87872	
100	400	1.2us	-144.4679dBc/Hz @10MHz	0.178	1.10004	
125	500	980ns	-145.7717dBc/Hz @10MHz	0.134	0.82812	
150	600	880ns	$\begin{array}{c} -145.8564 \mathrm{dBc/Hz}\\ @10\mathrm{MHz} \end{array}$	0.119	0.73542	
200	800	420ns	-144.3804dBc/Hz @10MHz	0.113	0.69834	
Assume the Bit error ratio is 10^{-3}						



On-going work: Rad-Hard Optical Transmitter

- 28nm CMOS 100Gb/s Optical transmitter is currently under work at Alphacore
- Optical transmitter/transceiver needs in the community ?



Summary

- This presentation introduced Alphacore's silicon-evaluated ADCs and other IP relevant to Nuclear Physics and High Energy Physics researchers.
- Please contact Alphacore for additional information about IP and IC availability, test results, evaluation boards, configuration, pricing, etc.
- Alphacore is looking for opportunities to optimize these readout solutions for your specific applications



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Questions?

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