Streaming readout of sPHENIX MVTX and R&D for EIC

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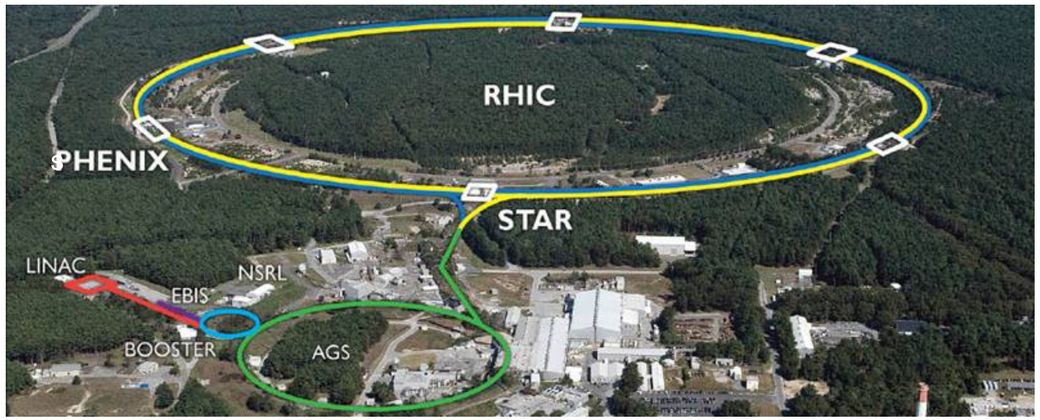
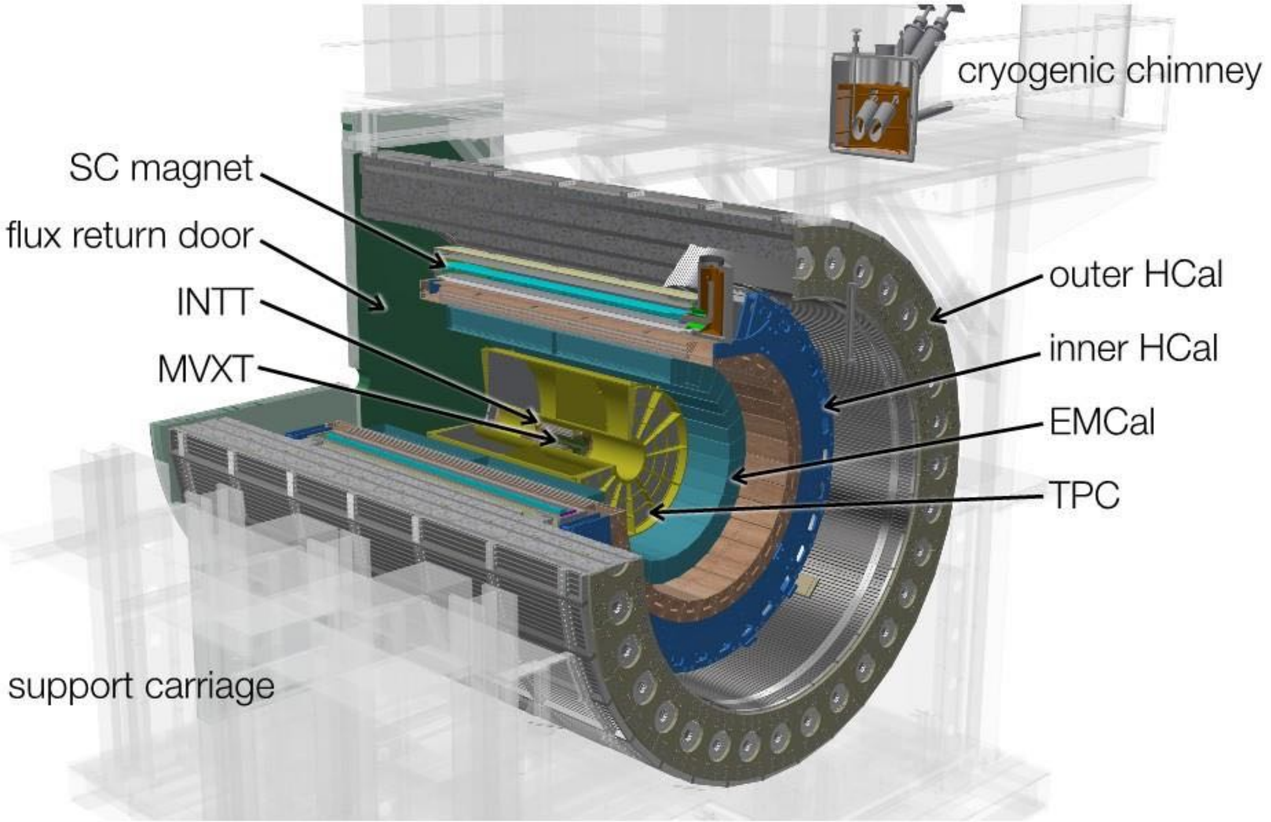
Workshop VIII on Streaming Readout

The sPHENIX Detector

- Super Phenix (sPHENIX) is a hermetic detector designed to study heavy flavor and jet physics in Heavy Ion Collisions at RHIC:
  - First run year 2023
  - High data rate (AuAu): 15 kHz for all detectors
  - N (AuAu) ~ 1.43 x 10^{10} (projection in 3 years of running)
  - 1.4 T magnetic field (reuse of old BarBar solenoid)
  - $|\eta| < 1.1$
  - High resolution vertexing with MVTX





sPHENIX Tracking Detectors

- Tracking currently consists of 3 sub-detectors:
  - MVTX: Monolithic Active Pixel Sensors (3 layers)
  - INTT: Intermediate Silicon Tracker (Strip Si)
  - TPC: Time Projection Chamber

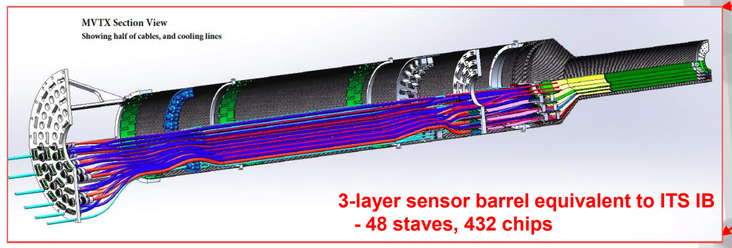
sPHENIX - MVTX

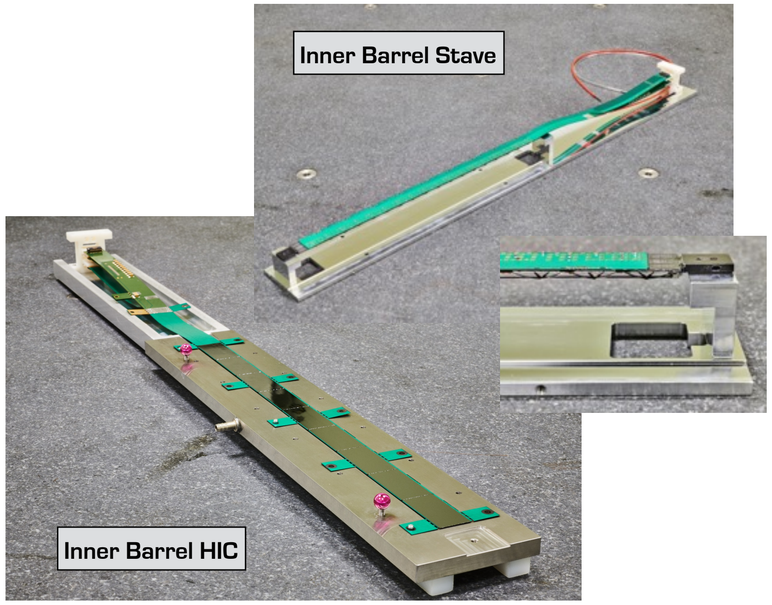
MVTX:

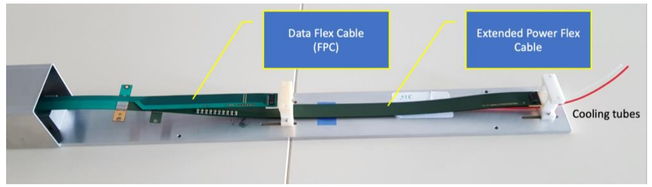
- 3 active layers (48 staves)
- 9 ALPIDE chips per stave
- Stave length: 290 mm
- Distance from IP: 2.5 – 4.0 cm
- Full azimuthal coverage: 2π
- $|\eta| < 1.1$

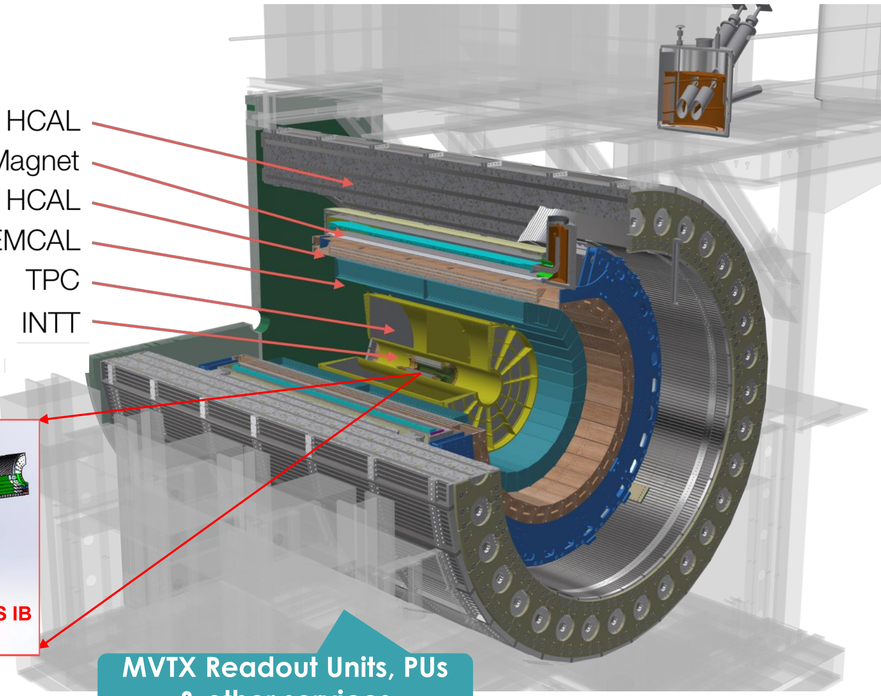
MVTX parameters: L = 271 mm

	R_min (mm)
Layer 0	24.61
Layer 1	31.98
Layer 2	39.93









Located Outside Magnet on Platform:
Much lower Radiation than ITS

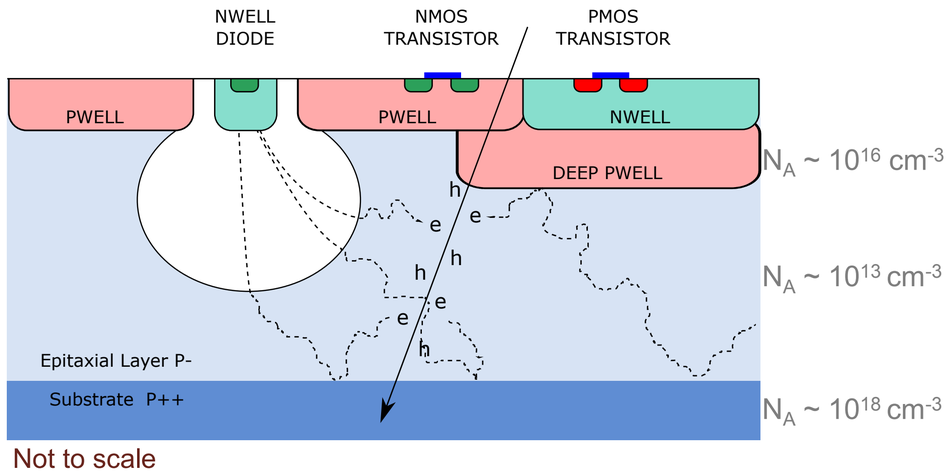
Staves are identical to ALICE ITS inner barrel staves, except for power leads

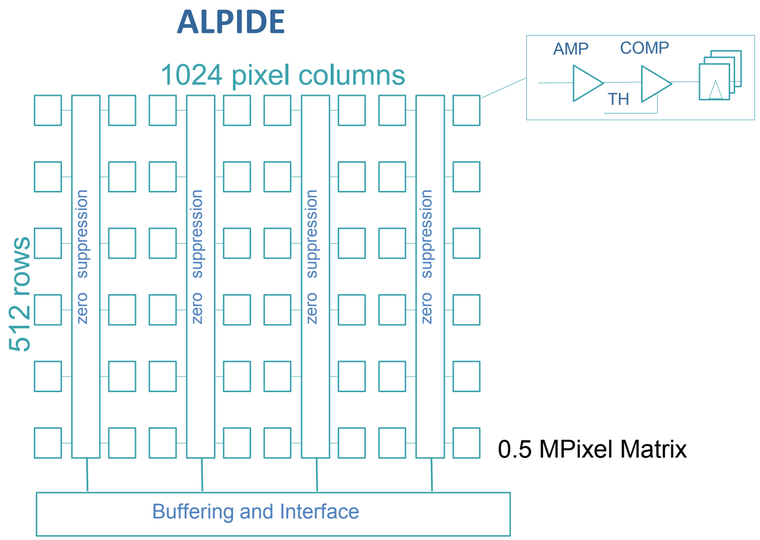
Produced at CERN and shipped to LBNL for test and assembly

ALPIDE Sensor Technology

Pixel Sensor CMOS 180 nm Imaging Process (Tower Jazz)

3 nm thin gate oxide, 6 metal layers

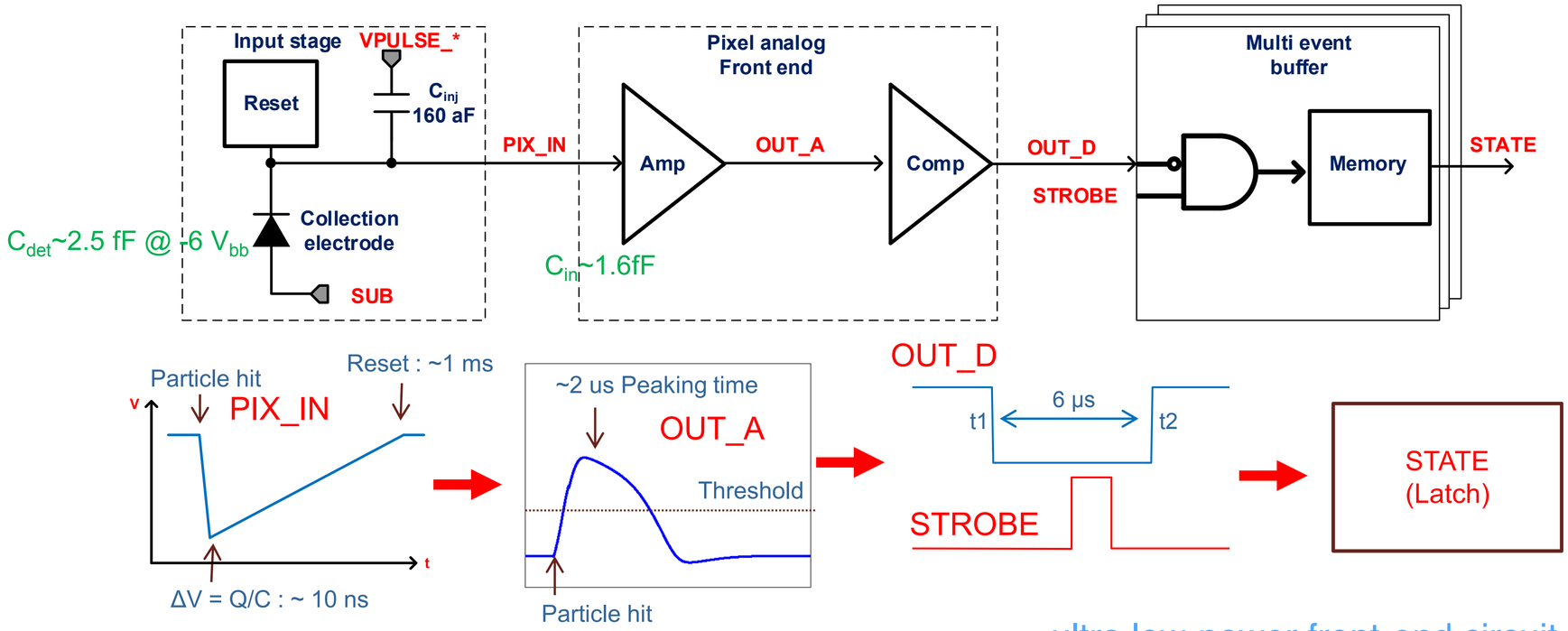




Key Features:

- 29 µm x 27 µm pitch, chip size 30 mm x 15 mm, 50 µm thickness
- High-resistivity (> 1 kOhm/cm) p-type epitaxial layer (18 µm to 30 µm) on p-type substrate
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel => low capacitance => large S/N
- Reverse bias can be applied to the substrate to increase the depletion volume around the N-well collection diode
- Continuously active, ultra-low power front-end (40 nW/pixel)
- Ultra-low power matrix readout (< 200 mW whole chip)
- High speed output serial link: 1.2 Gbit/s

ALPIDE Principle of Operation



ultra low-power front-end circuit

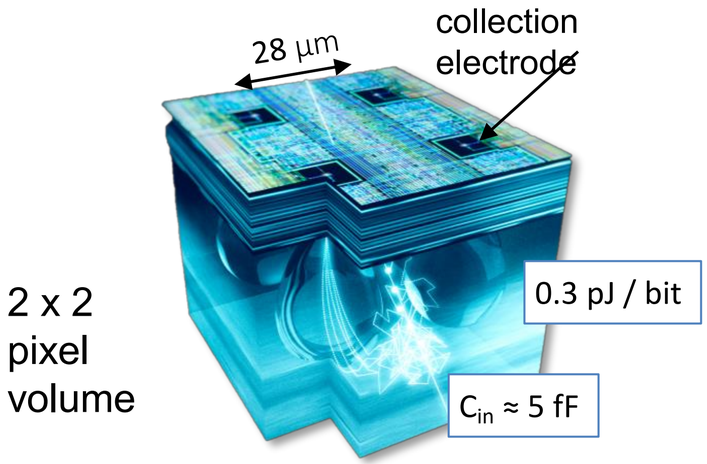
40 nW/pixel

Front-end acts as delay line:

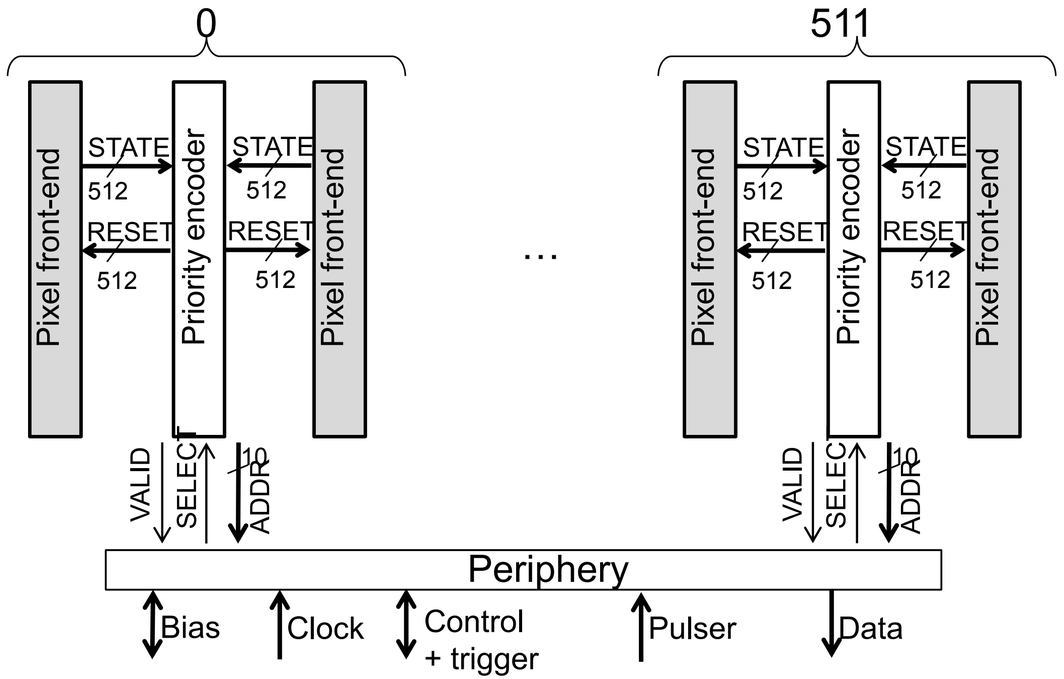
- Sensor and front-end continuously active.
- Upon particle hit front-end forms a pulse with ~1-2μs peaking time ("analogue delay")
- Threshold is applied to form binary pulse
- Hit is latched into memory if strobe is applied during binary pulse

Matrix Readout

3D - Charge collection features



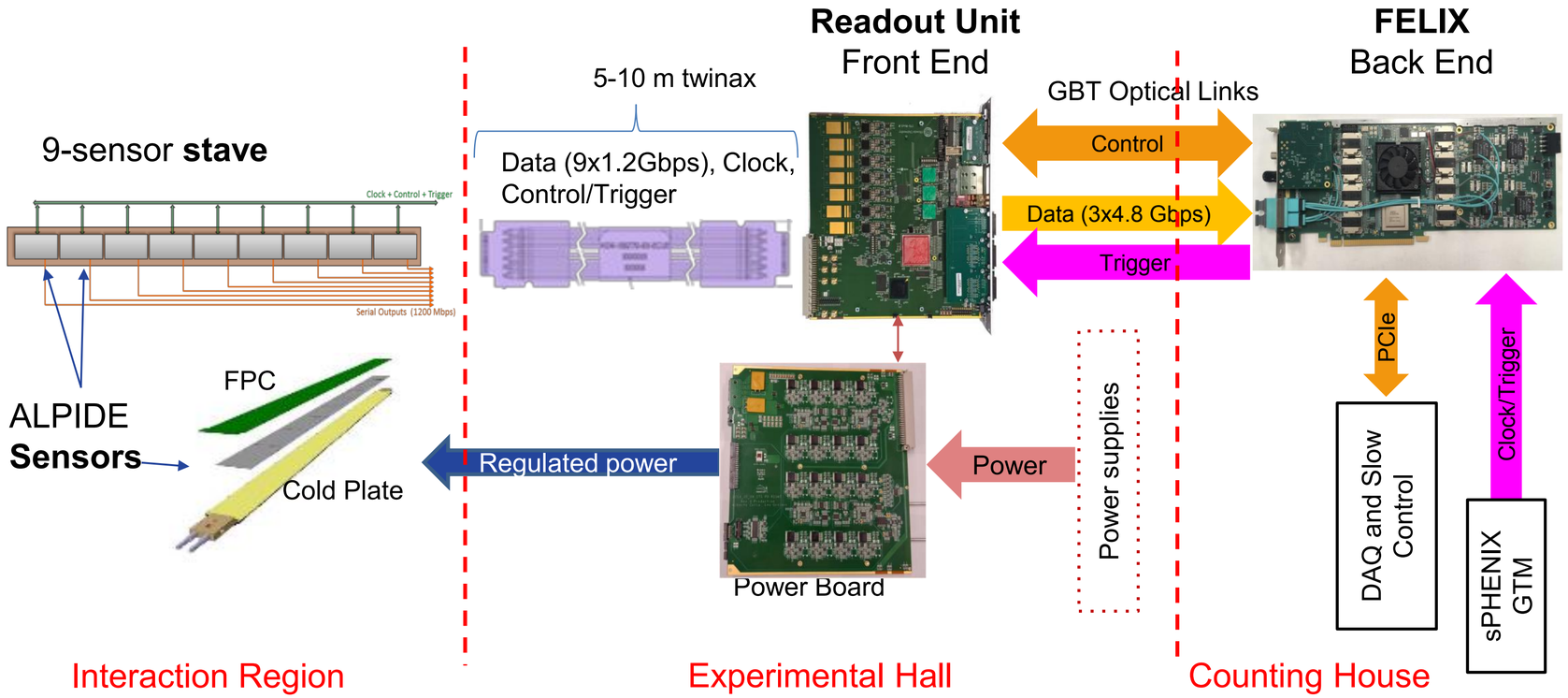
Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV



Pixel Matrix - Hit driven architecture

- Priority encoder sequentially provides addresses of all hit pixels present in double column.
- No activity if not hit (no free running clock) → low power

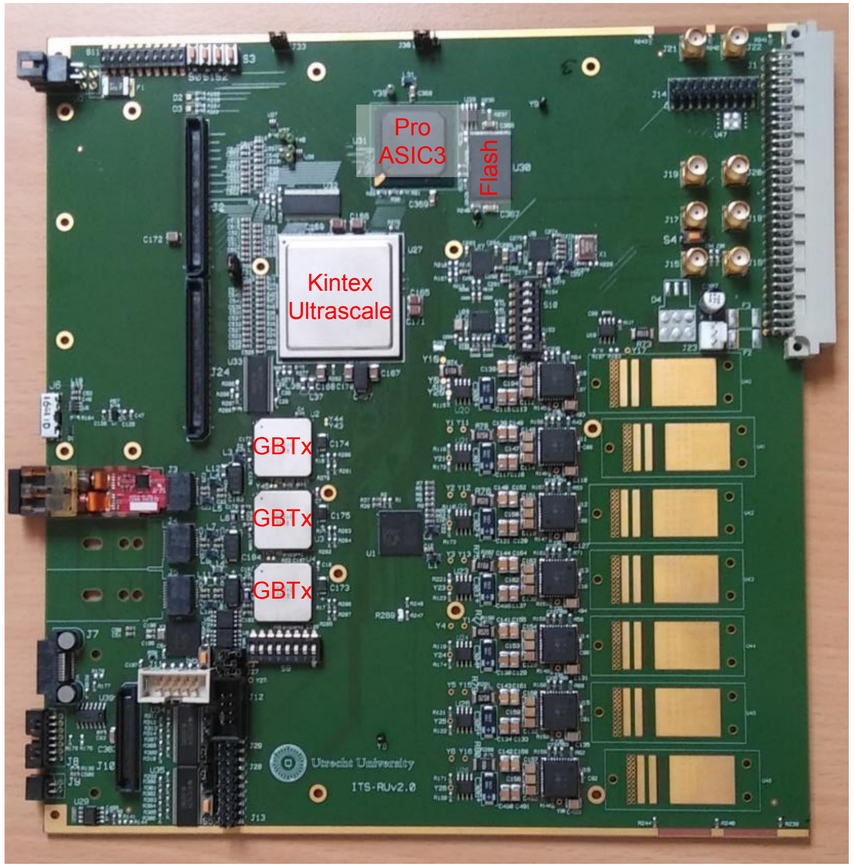
MVTX Readout Integration

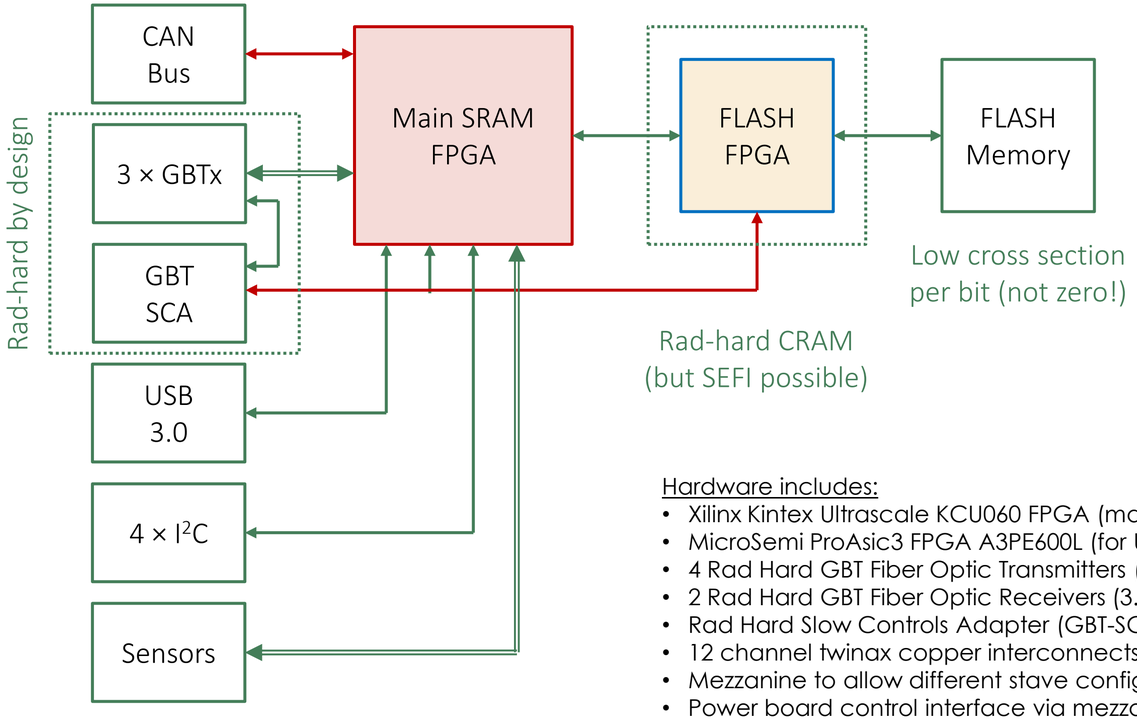


FELIX and Readout Unit are integrated: FELIX forwards trigger information and aggregates RU data.

- One Readout Unit (RU) per stave, 48 total
  - 9 x 1.2 Gbit/s firefly links, 1 clock, 1 control
  - 3 GBT optical links to FELIX per RU
- 8 RU per FELIX, 6 FELIX in total
- One Power Board (PB) supports 2 staves

Readout Unit from ALICE





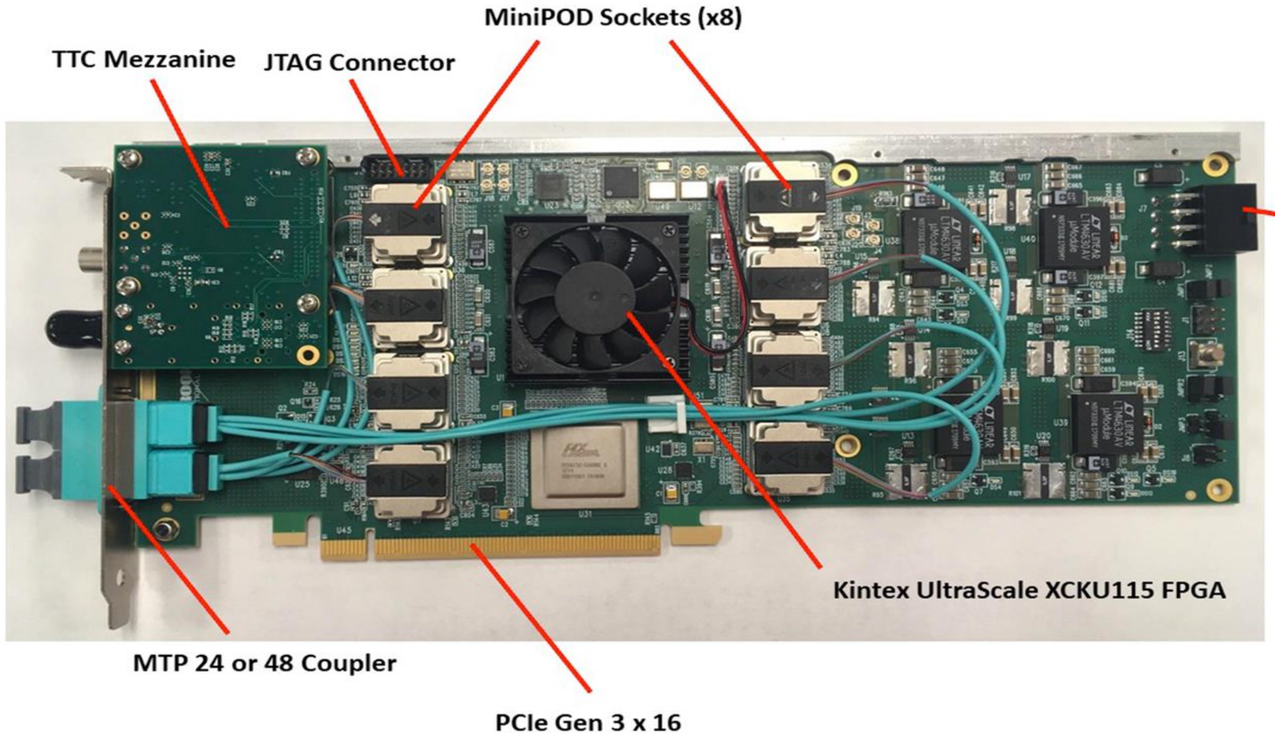
Hardware includes:

- Xilinx Kintex Ultrascale KCU060 FPGA (main programmable logic device)
- MicroSemi ProAsic3 FPGA A3PE600L (for Ultrascale scrubbing & configuration)
- 4 Rad Hard GBT Fiber Optic Transmitters (3.2 Gb/s each)
- 2 Rad Hard GBT Fiber Optic Receivers (3.2 Gb/s each)
- Rad Hard Slow Controls Adapter (GBT-SCA) for monitoring and control
- 12 channel twinax copper interconnects to stave
- Mezzanine to allow different stave configurations (“transition board”)
- Power board control interface via mezzanine
- CANbus interface as power board interface in case GBT is not available

➢ Controls the sensors, supplies them with clock and triggers.

➢ Retrieves data from sensors, formats them and optimizes data packets for GBT transmission to FELIX card.

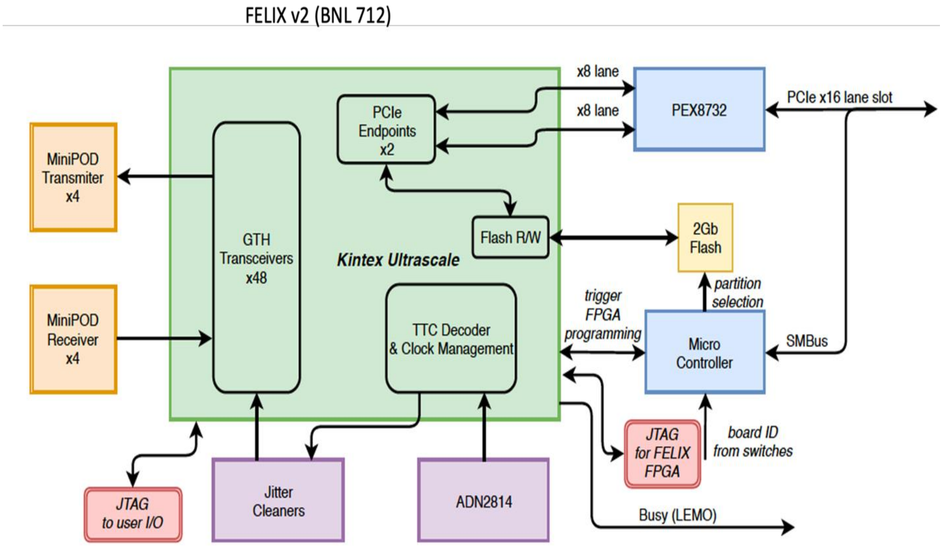
sPHENIX - MVTX "BackEnd": ATLAS FELIX



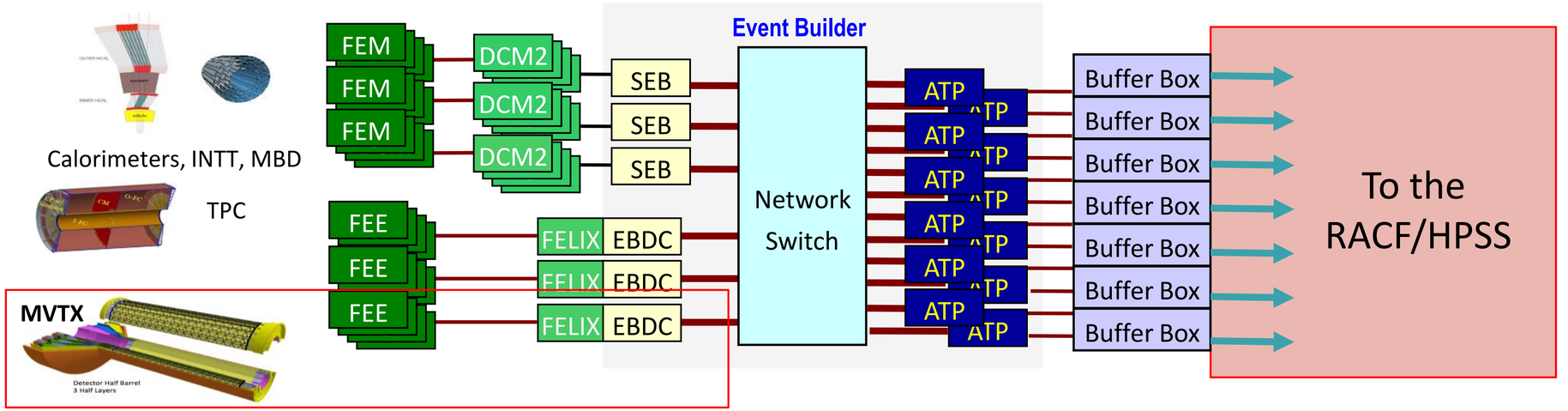
sPHENIX Timing Mezzanine

Architecture Highlights:

- Xilinx Kintex Ultrascale KU115 FPGA
- 48 bi-directional GBT links
- 16 lane Gen 3 PCIe
  - PCIe Tx > 100 Gb/s
- Mezzanine site for sPHENIX timing system card



sPHENIX DAQ Architecture



MVTX Hardware:

- 48 Staves
- 48 FEE (Readout Units v2.0)
- 6 FELIX v2.0
- 6 EBDC servers

Acronyms:

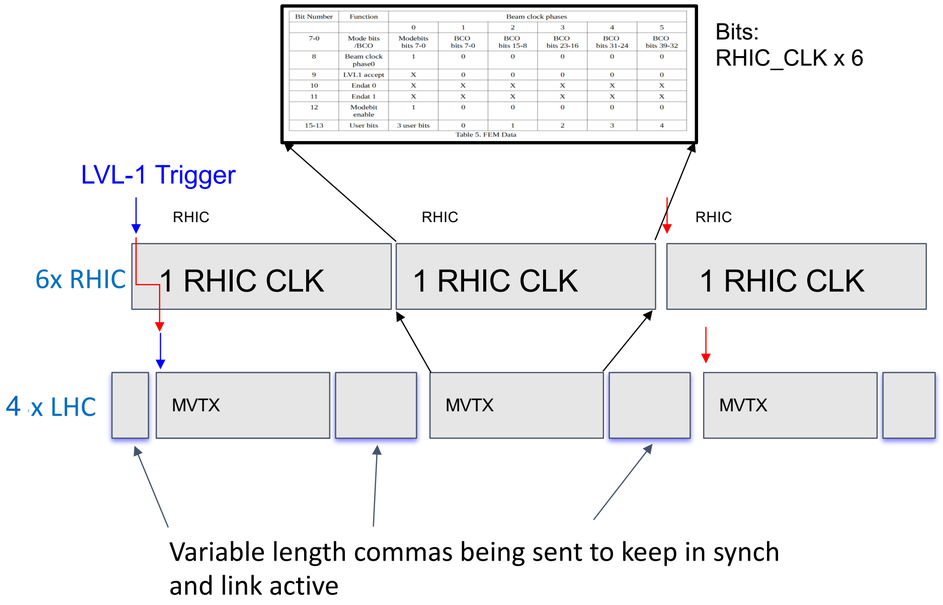
FEE	Front End Electronics
FELIX	Front End LInk eXchange
EBDC	Event Buffer and Data Compressor
ATP	Assembly and Trigger Processors
Buffer Box	Interim storage
FEM	Front End Module
DCM2	Data Collection Module
SEB	Sub-Event Buffer

MVTX will be integrated into the sPHENIX DAQ: working prototype of rcdaq plugin for FELIX and online data decoding/monitoring of ALPIDE data.

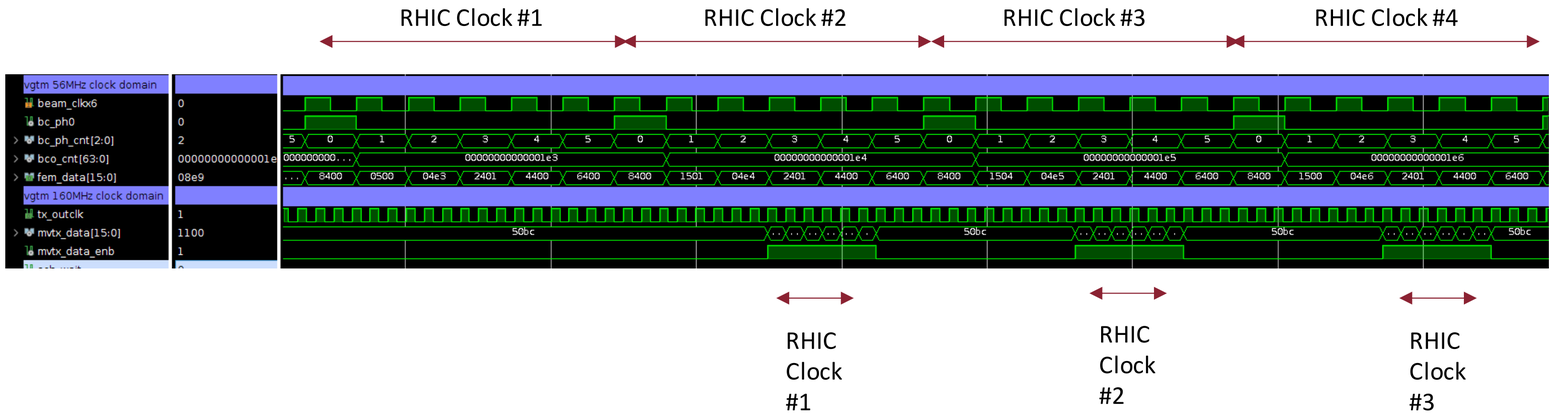
MVTX Trigger Timing System (mGTM)

- sPHENIX Global Timing Module (GTM) delivers a true 6x RHIC (9.4 MHz) clock to carry the timing information.
- Due to RU architecture (with the currently produced RU) MVTX system needs a 40.079 MHz clock for the operation of the GBTx ASICs.
- We need one unique clock going to all six FELIX, which sends a derivative to the RU and eventually to the ALPIDE.
  - Only way to keep MVTX synchronized

Proposal is to send data to MVTX at a higher frequency, adding comma's into extra clock cycles to keep the two data rates close in time



- All GTM information is received within one RHIC clock
- RHIC clock is divided into 6 phases for GTM data transmission
  - Get about 17 clock edges at 160 MHz rate for each RHIC clock
- Due to added pipeline delays from the FIFO, the trigger latency is increased by about 140 ns

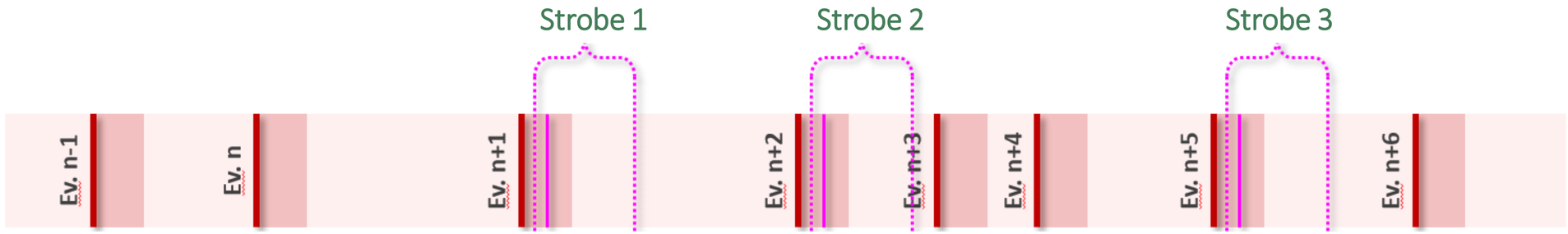


Triggered and Continuous mode operations

The MVTX can operate in two modes:

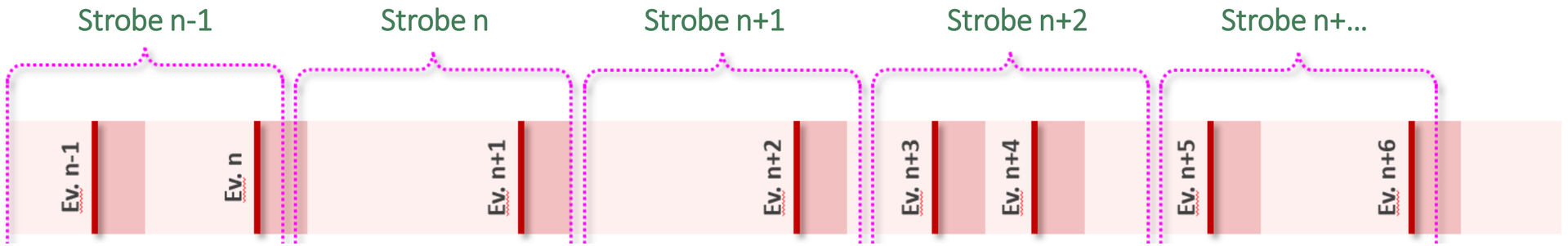
Triggered mode: Pixels are latched with a short strobe window, followed by read out, based on an external trigger.

e.g. Physics trigger (with latency ~ 6 μs) in the trigger word from sPHENIX GTM data.

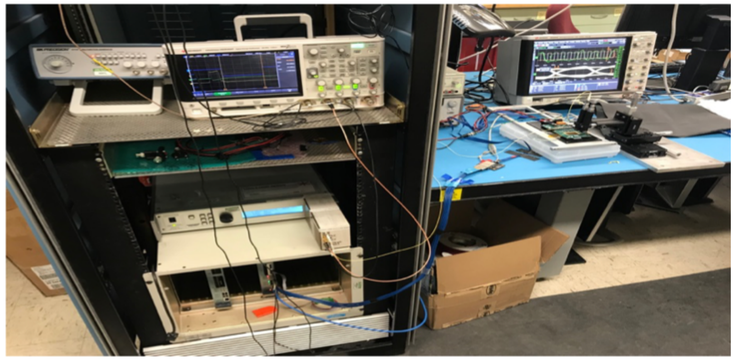


Continuous mode: Pixels are latched using long, periodic strobe windows with short inter-strobe periods (~100 ns) to initiate readout.

e.g. every orbit with the length of an orbit (120 x 106 ns = ~ 12 μs)



Trigger Latency Study

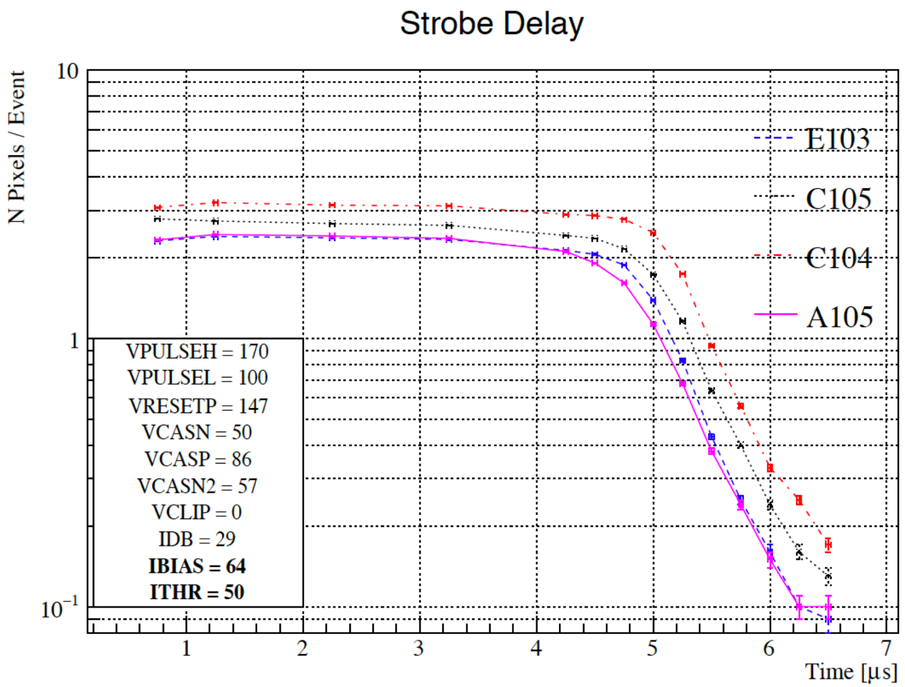


Study ALPIDE performance with Pulsed Laser @ LANL

- Inject "MIP" signal:
  - 850 nm laser, 4 ns wide pulse, ~1 MIP
  - 50kHz trigger
  - Find optimal MAPS operating parameters

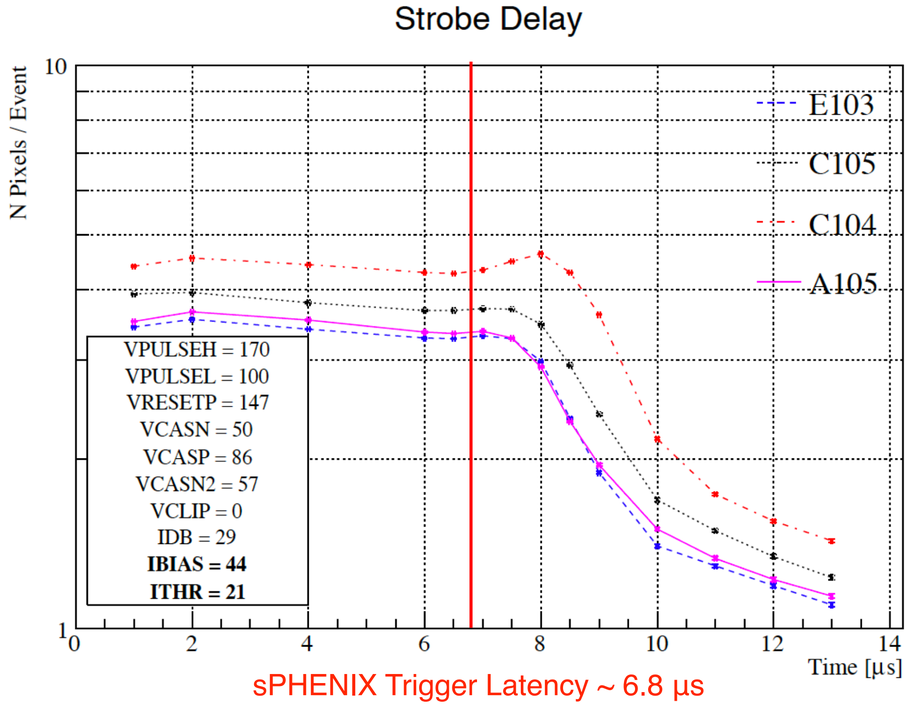
ALPIDE Default Settings

Integration time ~ 5 µs



"Stretched Settings" for sPHENIX trigger study

Integration time ~ 8 µs



sPHENIX Trigger Latency ~ 6.8 µs

Streaming Readout and Per-strobe ALPIDE multiplicity

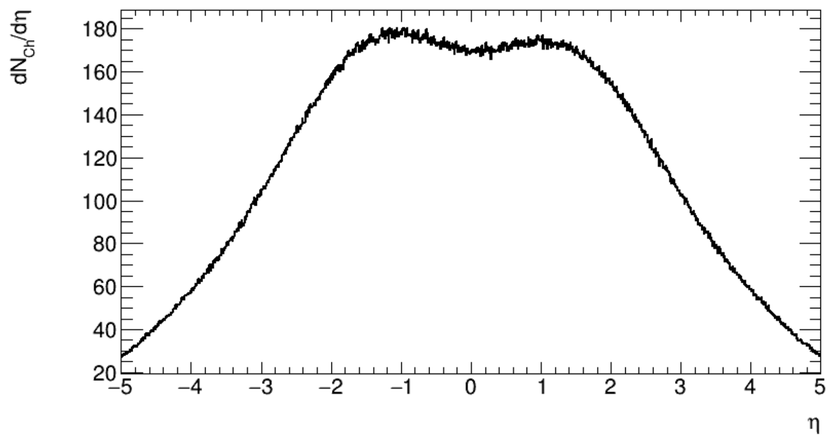
Continuous Readout is preferred:

- In order to decouple the analogue shaping time tuning from the sPHENIC global trigger latency choice.
  - e.g. Preserving the important tune of the threshold setting.
- In addition, running all inner tracking system (MVTX, INTT and TPC) in continuous readout mode will record 500x higher statistics of M.B. p+p collisions
  - Which will improve the HF measurements in the central kinematic region.

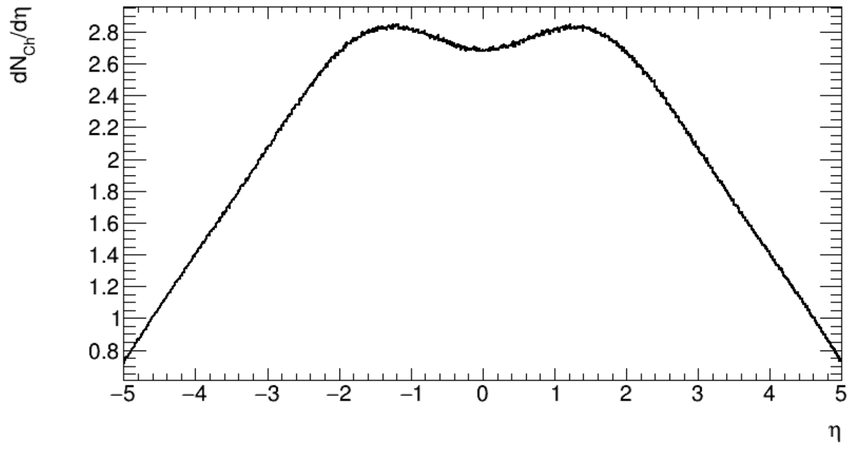
Several factors contribute to the per-strobe multiplicity for a given ALPIDE pixel in a MC simulation:

- Per-collision multiplicity (PDF used in the simulation)
- Number of pile-up collisions -> Poisson distributed
- Number of Noise hits (10^{-6}) -> Poisson distributed
- Duplicated hits, due to the integration time of the front-end, are included in the next integration window

HIJING M.B. Au+Au



Pythia8 M.B. p+p

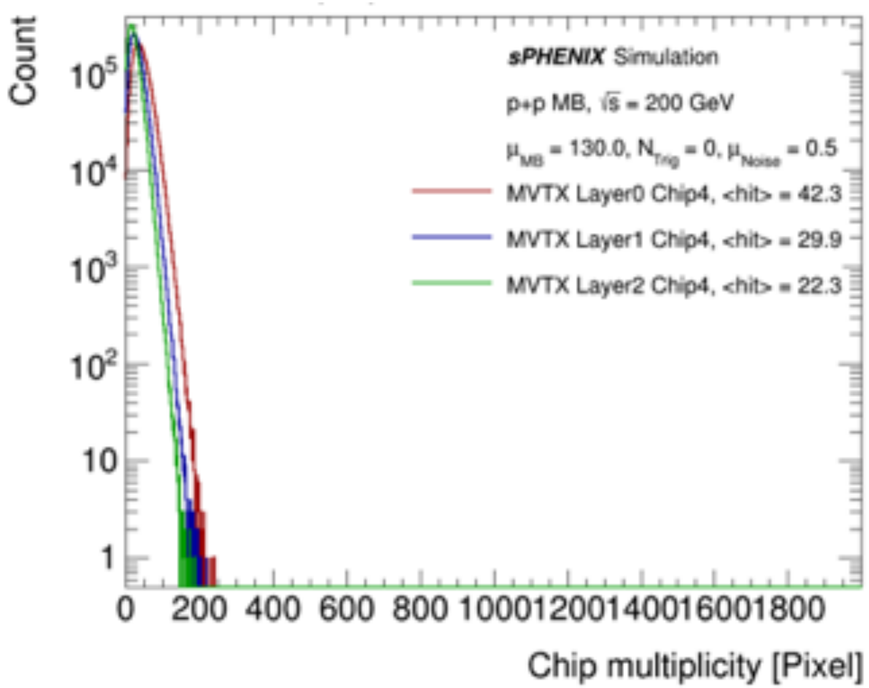


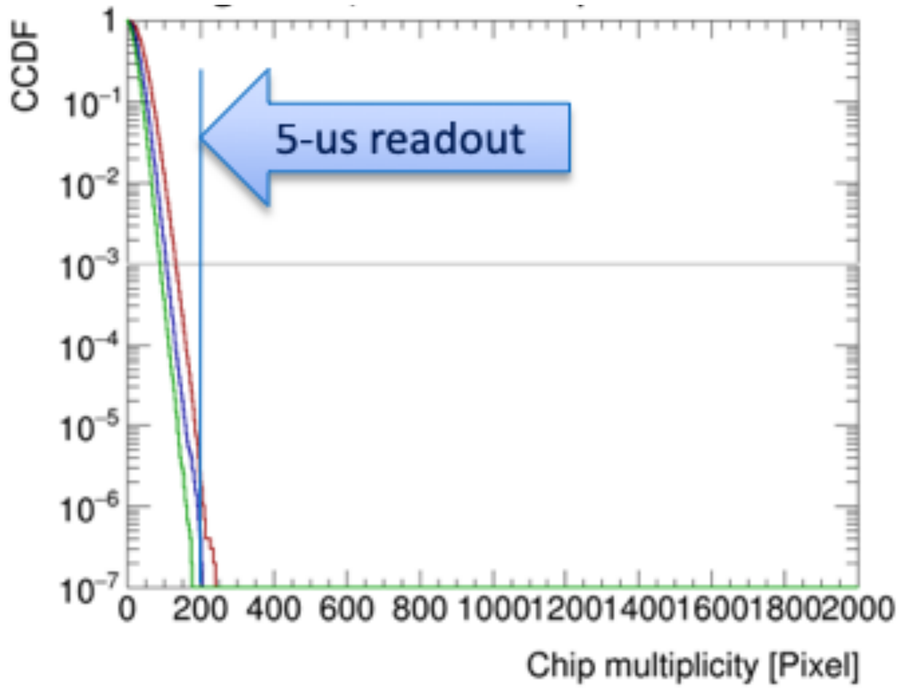
p+p multiplicity, per-strobe, chip-4

Continuous-mode is plausible at 5-us strobe window too

➢ Probability [readout-time per strobe > 5 μs] < 10^{-5}

13 MHz p+p collisions, 10-μs strobe width + 5-μs integration, 10^{-4} noise per strobe

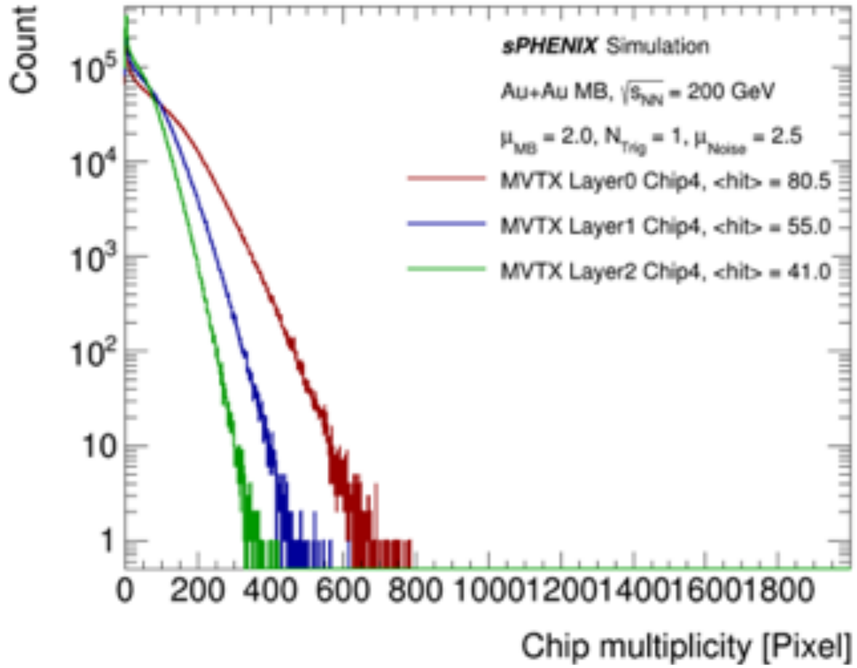


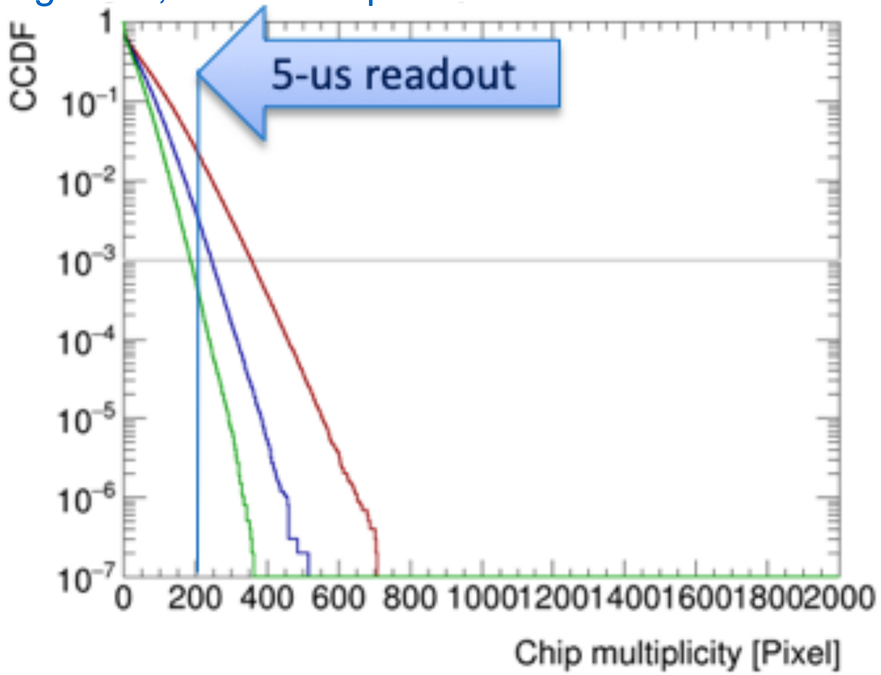


Au+Au multiplicity, per-strobe, chip-4

- Reducing integration windows to 5 μs is trickier for Au+Au collisions, due to high fraction of noise and higher fluctuation in pileup
- Percent-level chance that 3rd buffer is needed to avoid the loss.

200 kHz Au+Au collisions, 5μs strobe width + 5-μs integration, 10^{-4} noise per strobe

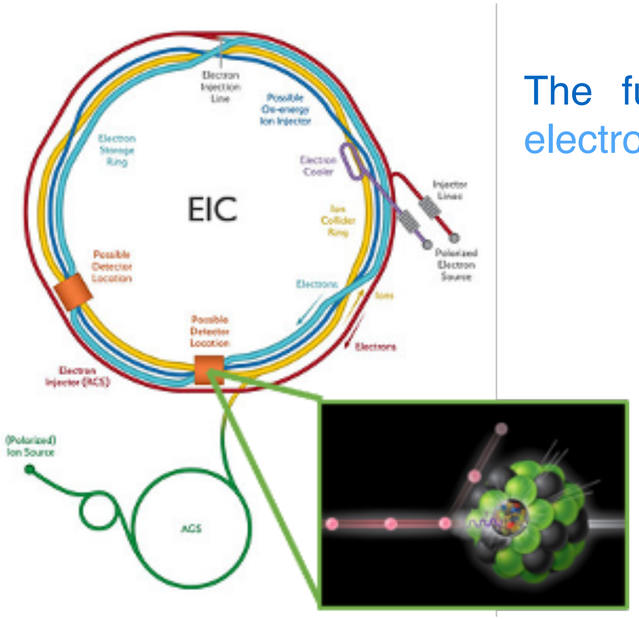




Caveat:

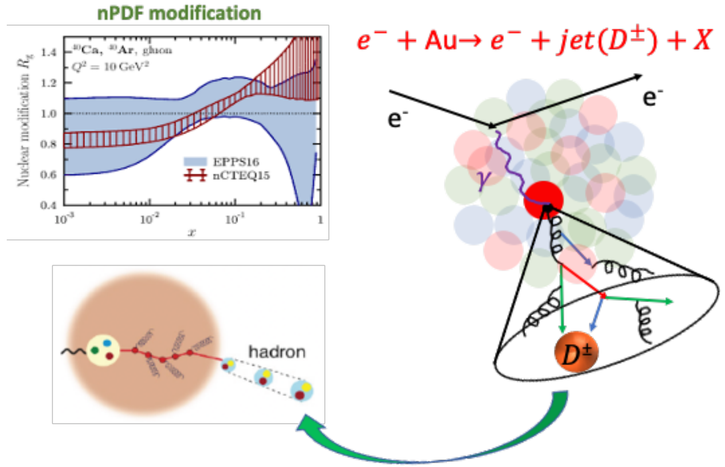
- All discussion is driven by the tails of the distribution which need to be well understood.
- Plus a detailed simulation of the data flow and the instantaneous rates.

What's next: LANL Forward Silicon Detector proposal for the EIC

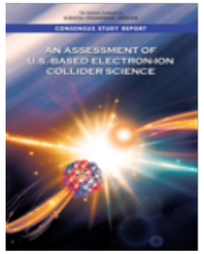


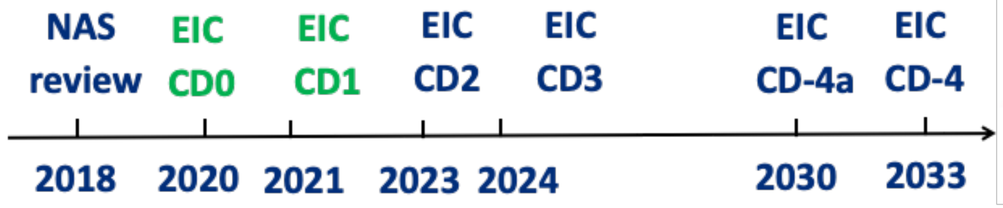
The future Electron-Ion Collider (EIC) will utilize high luminosity high energy electron+proton and electron+nucleus collisions to solve several fundamental questions.

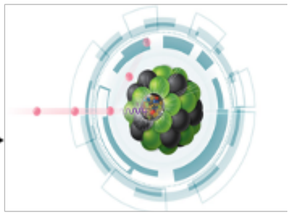
- Through measuring heavy flavor hadrons, jets which can be treated as surrogates of initial quarks/gluons and their correlations in the hadron/nuclei going (forward) direction in e+p/A collisions at the EIC.



- To understand the nuclear medium effects on hadron production such as 1) modification on initial nuclear PDFs and 2) final state hadronization processes through the comparison of measured heavy flavor hadron/jet cross section between e+p and e+A collisions.



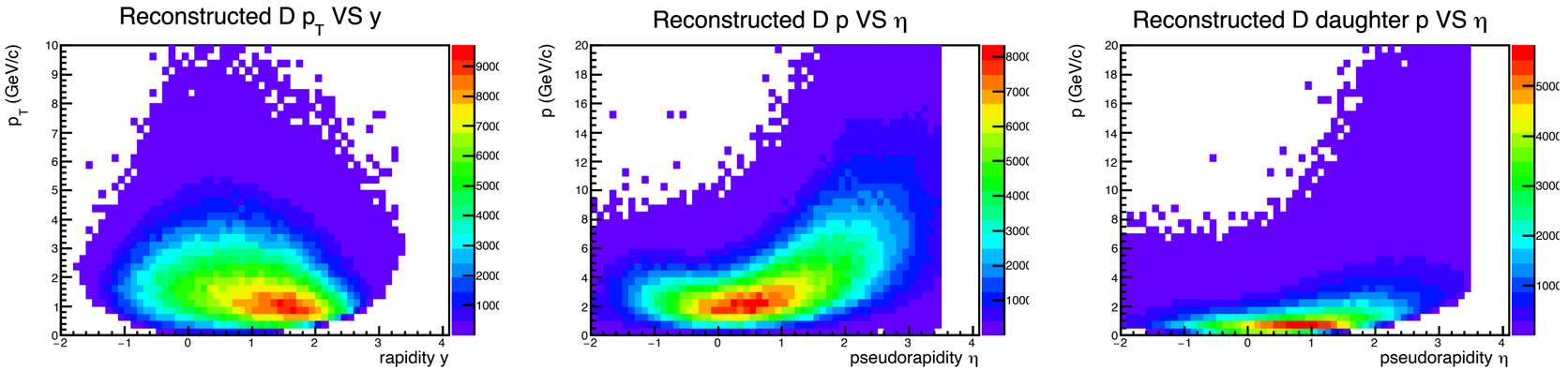




Requirements for a silicon vertex/tracking detector at EIC

- To meet the heavy flavor physics requierements, a silicon vertex/tracking detector with low material budgets and fine spatial resolution is needed

- Particles produced in the asymmetric electron+proton and electron+nucleus collisions have a higher production rate in the forward pseudorapidity. The EIC detector is required to have large granularity especially in the forward region.



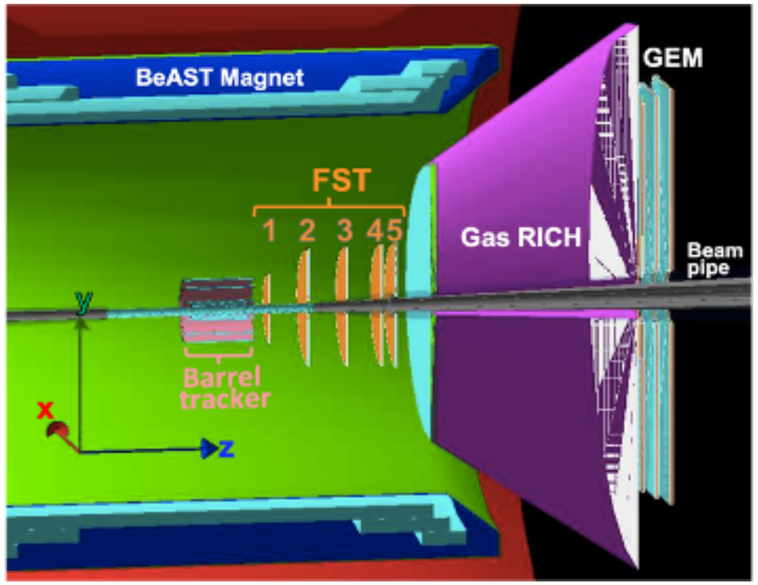
- Fast timing (1-10ns readout) capability allows the separation of different collisions and suppress the beam backgrounds.

Conceptual design of the proposed FST detector

- In GEANT4 simulation with the Fun4All (sPHENIX and EIC simulations) framework:
  - The proposed Forward Silicon Tracking Detector (FST) consists of 3 planes of MAPS silicon detector and 2 forward planes of High Voltage (HV)-MAPS silicon detector.
  - R&D for all possible silicon sensor options in progress:
    - LGAD, AC-LGAD, MALTA are under R&D at LANL -> exploring the readout options
    - First studies focussed on the tracking spatial resolution performance
    - More realistic/complete description will be implemented in the simulation once the results from R&D characterizations are available.

LANL FST integrated inside the EIC

Different detector designs documented in arXiv:2009.02888

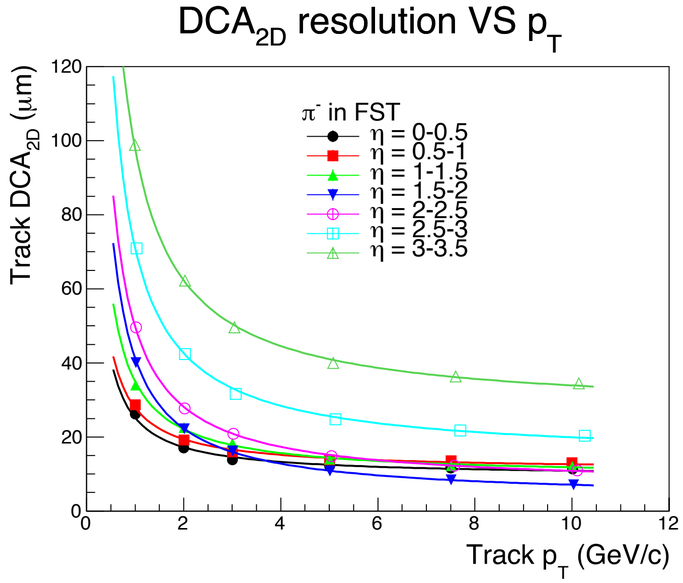


Silicon sensor options

	Pixel pitch	Silicon thickness	Integration time
LGAD/AC-LGAD	100μm	<300μm (<1% X_0)	300-500ns
MALTA (Implemented in simulation)	36.4μm	100μm (<0.5% X_0)	5ns
ITS-3 type	20μm	50μm	100ns ?

"These studies are supported by LANL LDRD 20200022DR project"

LANL FST help determine the track Distance of Closest Approach(DCA) with good precision!



Summary

- MVTX plans to operate in Continuous readout mode from Day-1:
  - MC simulations have shown that continuous readout mode for MVTX detector is plausible.
  - Continuous readout avoids dead-time and biases due to standard triggering techniques

- Silicon MAPS is recognized as a leading technology for EIC detector applications.
  - LANL FST proposal will have a great impact to the Heavy Flavor physics at EIC detector.

Thank you for your attention