CLAS12: from triggered to free running DAQ

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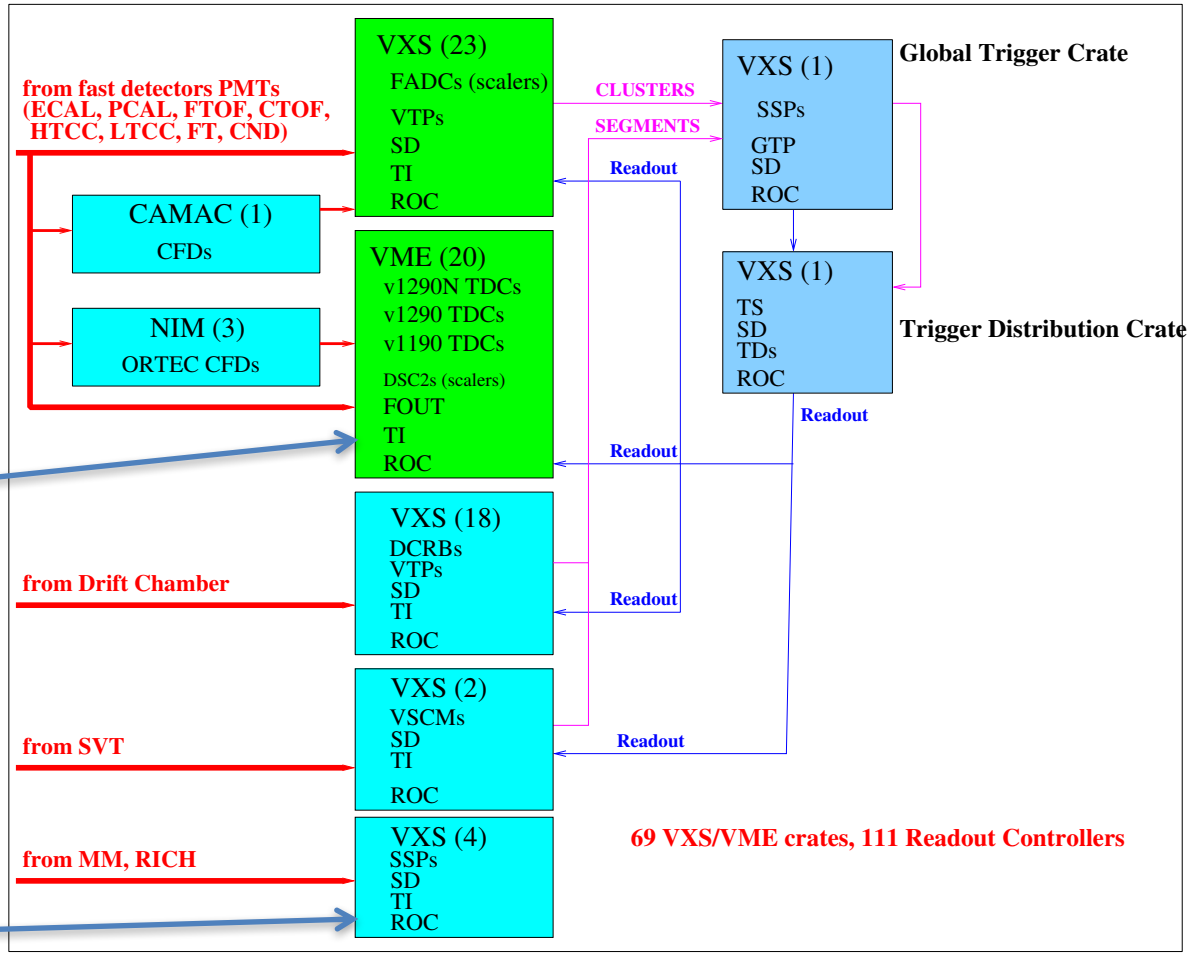
Workshop VIII on Streaming Readout

April 28, 2021

1. Front End Electronics Upgrade
2. Trigger System Evolution
3. Streaming Readout

CLAS12 front-end upgrade for 100kHz – and for streaming



Upgrade VME to VXS crates with VETROC TDCs

MM readout based on VMM3/Sampa ASIC

VME to VTP readout

VETROC TDC board

Channel counts:
- 64 channels on VETROC base; plus
- 64 channels on Mezz. Cards; plus
- 64 channels via VME P2/backplane IO card.
  --Any-level differential (converted to LVTTL on board)

Power supply:
- VME: +5V, +12V -12V

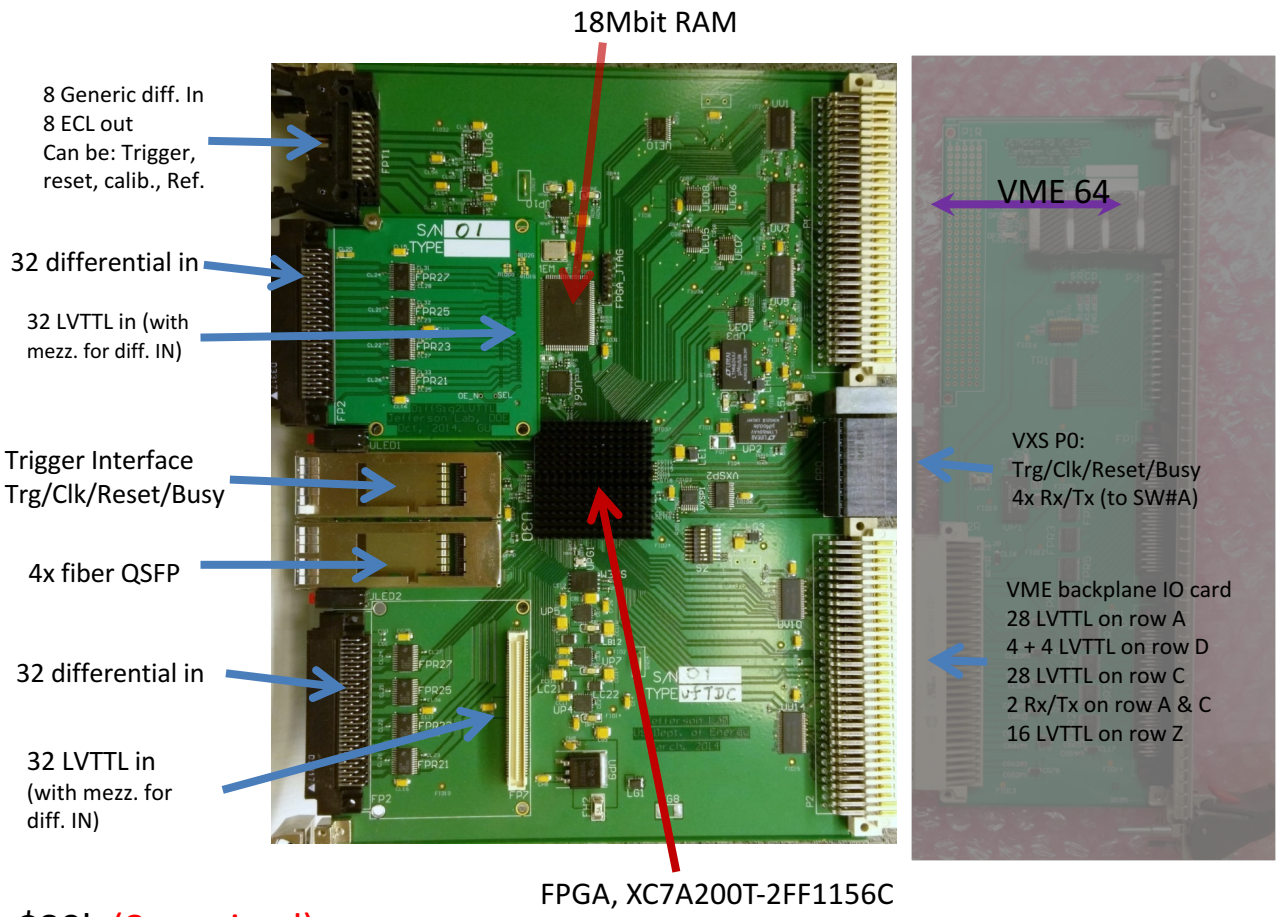
Data Readout:
- VME 64
- VXS P0
- QSFP front panel

Slow Controls(FPGA loading, setting etc.):
- VME for slow control

Fast Controls inputs (trigger etc.):
- VXS P0 (VXS payload slot);
- QSFP front panel (like a TI);
- Generic input (8-pair) front panel connector.

Measurement precision:
- ~ 35 ps, limited by the 'LVTTL' conversion

Status:
- Triggered readout: ready (both the FPGA firmware and the VME software)
- Streaming readout: FPGA firmware is available, but needs be tested



Budget: 40 VETROCs x $2k = $80k (8 received)

Crates VME64X->VXS backplane upgrades – 8 x $6.5k = $52k (6 installed)

1 new VXS crate (CTOF-HTCC separation) with CPU, SD, TI = $20k

Connectors, cables - $10k

Total: $162k

MM readout based on VMM3 ASIC

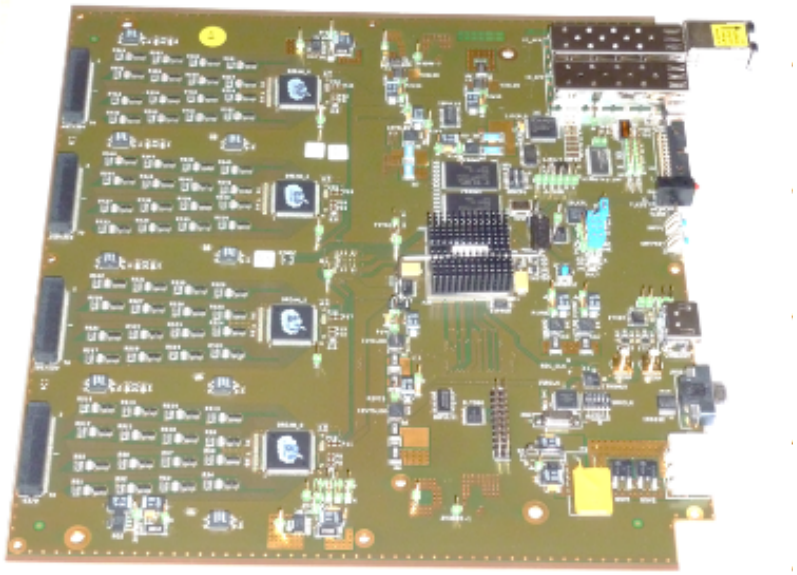


Figure 11: Photograph of the 512-channel Front-End Unit.

Notes:

1) **Trigger support would allow future expansion to support integration into trigger system. Requires a significant number of additional FPGA I/O, hence the increased FPGA costs for that configuration.**
2) **VMM3 noise & dynamic range still need to be confirmed suitable for use in CLAS12 MM use case**
3) **Backend may need a V**

FEU Replacement (DREAM -> VMM3A) Cost Estimate

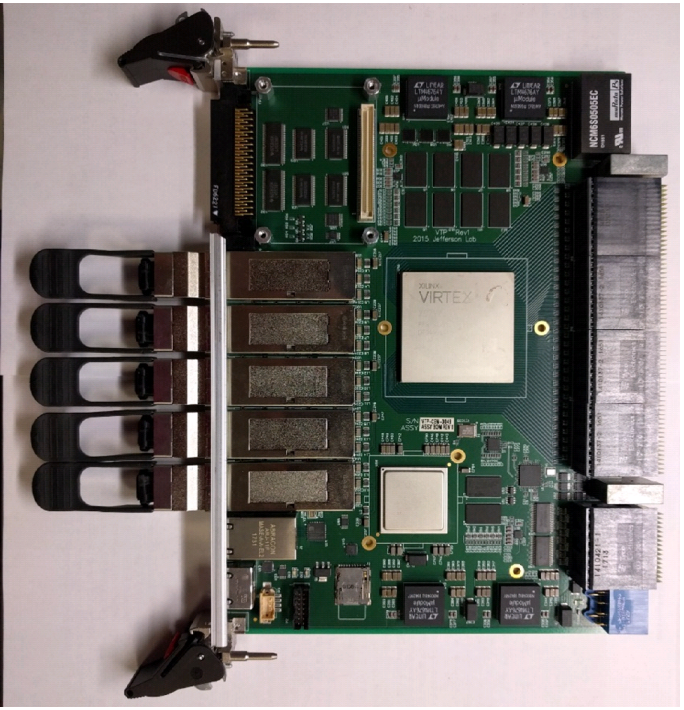
- 512 channels per board (8x DREAM -> 8x VMM3A)
- 12 FEU (FMT) + 36 (BMT) => 48 FEU boards needed
  (need to double check this is exactly right)
- 48 * 8 = 384 VMM3 ASICs
- Plan to use same detector connector and readout fiber (so this upgrade will only replace these boards). VTP will be required to bypass VME readout to achieve high performance: 10GbE readout with VTP would support full MM readout @ 100kHz with ~15% occupancy (assuming 32bit per hit)

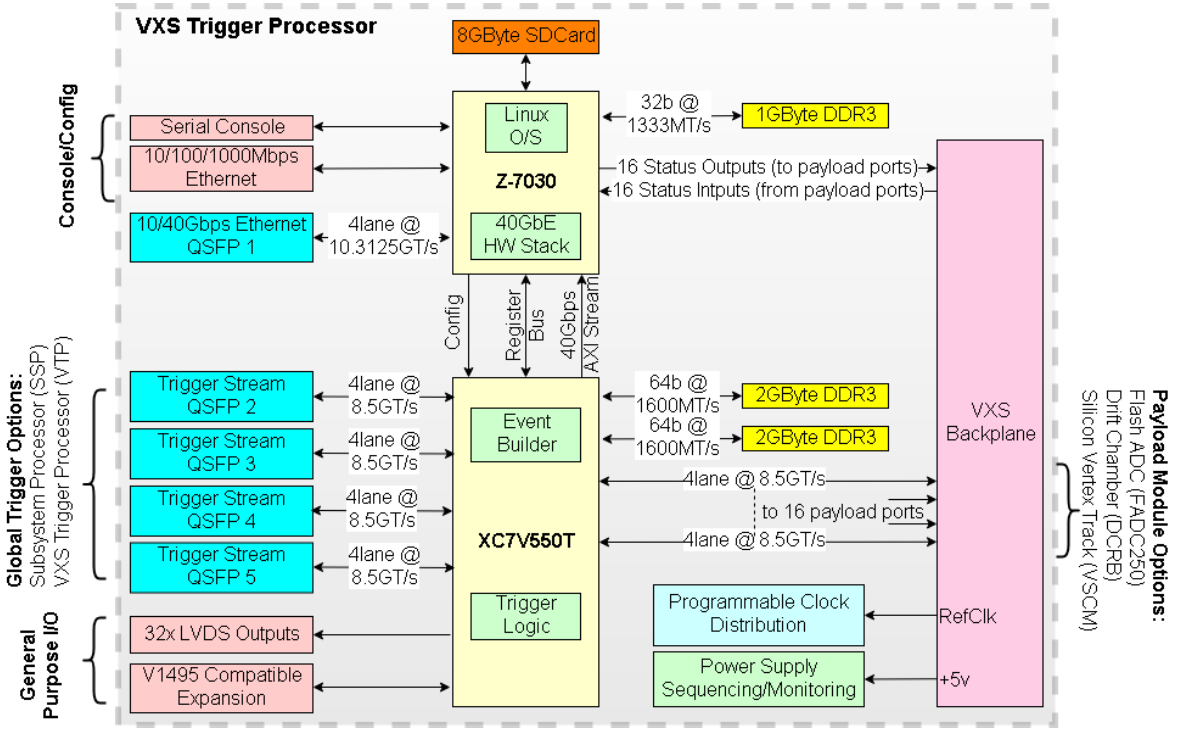
- Components
  - FPGA (if 6bit trigger path implemented): $1,000
  - FPGA (if only readout path implemented): $350
  - Connectors: $50
  - Fiber transceiver: $80
  - PCB: $300
  - Assembly: $500
  - ASIC (???): $800 (this assumes $100 per chip, online I've read $25 – probably depends on if we can piggy-back an order)
  - Misc (power, memory, etc): $200

- Unit cost (w trigger*, w/o trigger): $2930, $2280

- **Total (w trigger*, w/o trigger): $150k, $110k**

Upgrading VTP board for streaming readout





- In existing trigger-based mode, VTP sends trigger information from QSFP2 to the following trigger system stage, and will be able to act as readout board in the same time if needed (2.5->3.125 for serial on back plane, 10Gbit out from 16 slots); more VTPs may be needed if used for readout (MM)
- In streaming mode, there is no trigger information, VTP sends stream of data from QSFP1 to Linux server with expected bandwidth up to 4 x 10Gbit/s link
- FPGA based TCP/IP protocol is used between VTP and Linux server
- **Needs about 100K to read all VXS crates through VTPs instead of VME bus**

DAQ upgrade up to 100kHz event rate

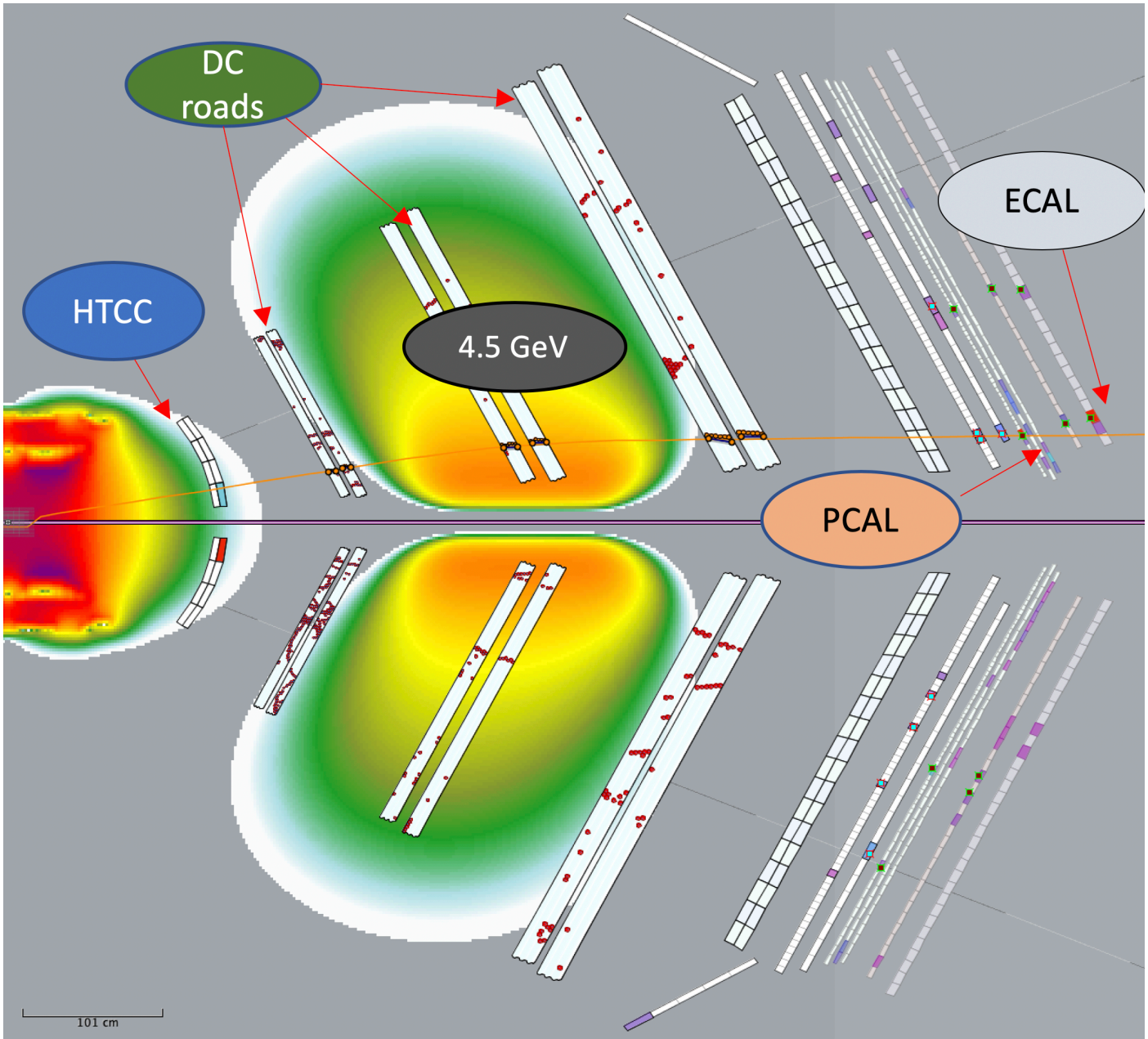
- Trigger-based mode is used
- FADC250, DCRB, VSCM, SSP boards will stay
- CAEN TDCs have to be replaced with VETROCs, VME crates to be converted to VXS
- MM readout to be decided, proposed solution is new VMM3 ASIC based board, work in progress with MM team
- SVT ASIC performance have to be validated for high luminosity running
- Some VTPs have to be used as both trigger and readout modules, firmware under development (reason is limited VME readout bandwidth)
- Some boards firmware and CODA software have to be validated and may need to be modified/fixed
- CODA software (EB in particular, also ET and ER) have to be able to process higher rate, may need improvements
- Work can be performed in steps, with partial performance improvement on every step
- Time scale 2 years

DAQ upgrade to streaming

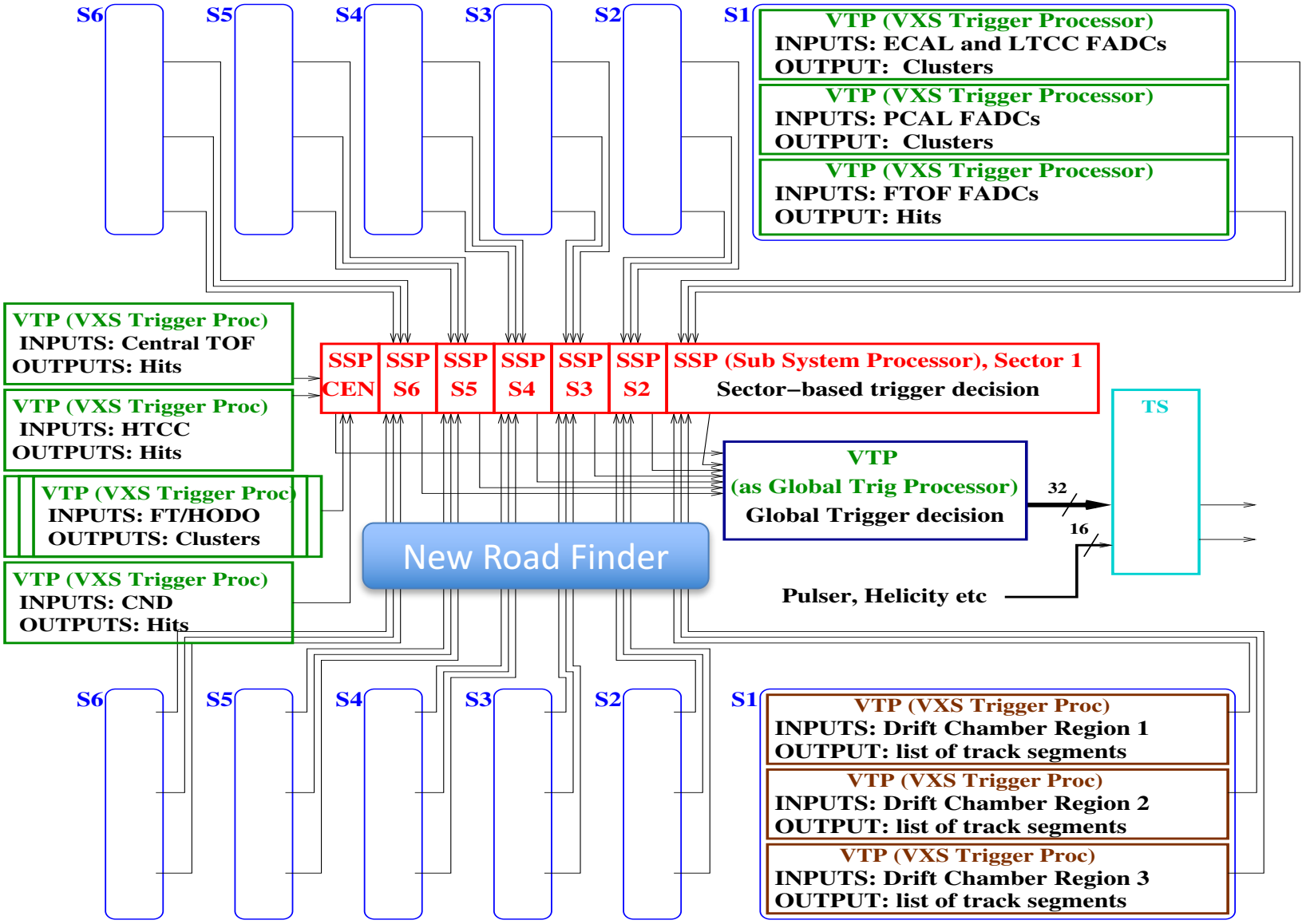
- VTP, FADC250, DCRB, VSCM, SSP, VETROC boards can be reused, or/and new non-vxs based electronics can be used
- Exact streaming DAQ configuration for CLAS12 to be decided during following years based on available technology
- All new electronics development (ASICs etc) have to be compatible with streaming mode
- New streaming version of CODA is needed – not available at current time, switching to streaming DAQ can be considered only when back-end is available or close to become available
- Time scale 3-5 years depending on demand

Front-end electronics upgrade to streaming mode is underway, no serious problems anticipated

CLAS12 Electron Trigger Event Example



CLAS12 Trigger System (level1)



CLAS12 Trigger System Status

- Fully operational, efficiency close to 100%
- Portion of 'good' events depends on trigger type (electron, photon, meson), about 50% in average
- The achieved performance of the CLAS12 Trigger System allows use without significant changes for the entire CLAS12 physics program

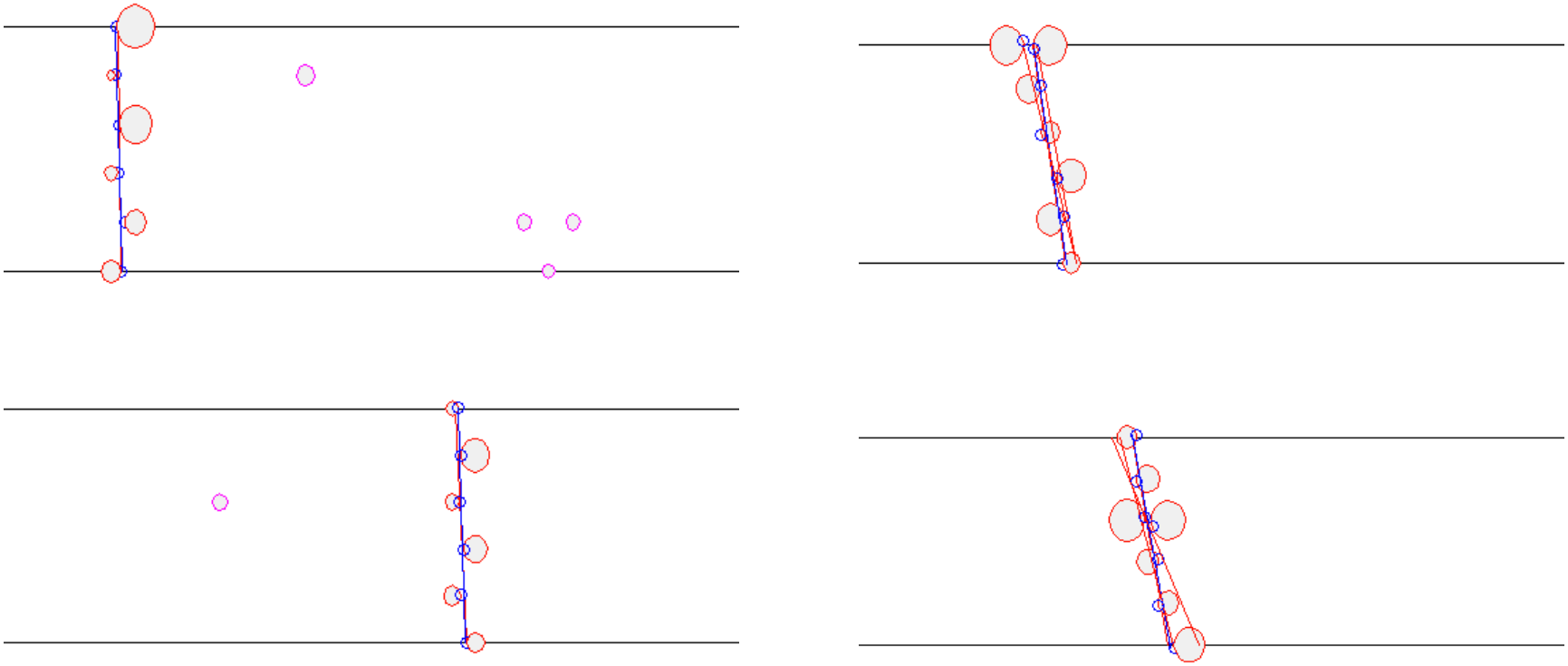
CLAS12 Trigger possible improvements

- ECAL/PCAL trigger can to be improved in following ways: (1) in addition to electron shower clustering, search for MIP-like clusters have to be added to improve muon class triggers; (2) use individual strip real attenuation length instead of average one; (3) allow individual strip timing delays and improve cluster timing reporting
- DC trigger can be improved (needed in particular for Q**2 cuts) in following ways: (1) segments selectivity and space resolution improvement; (2) roads space resolution improvement; (3) drift time usage to improve two previous items feather
- Additional geometry matching between detectors, for example DC vs PCAL clusters,
- Allow multi-particle trigger in one sector
- Improve timing coincidence by narrowing signals from different trigger components

CLAS12 Trigger Upgrade and path to the streaming daq data processing

- Current trigger system is solely based on FPGA, there is no Level3 component
- We decided do not touch existing Level1 trigger, and implement all additional elements in new level3 (software) trigger
- Dummy Level3 component was added, and all trigger improvements will be developed as Level3 elements; it will allow not only improve current trigger, but also develop solutions for future streaming DAQ data processing
- Initial tasks for level3 will be drift chamber segment finder, and AI-based track finder

CLAS12 Trigger, Drift Chamber Segment Finder
(works on 112x6 wire superlayers)

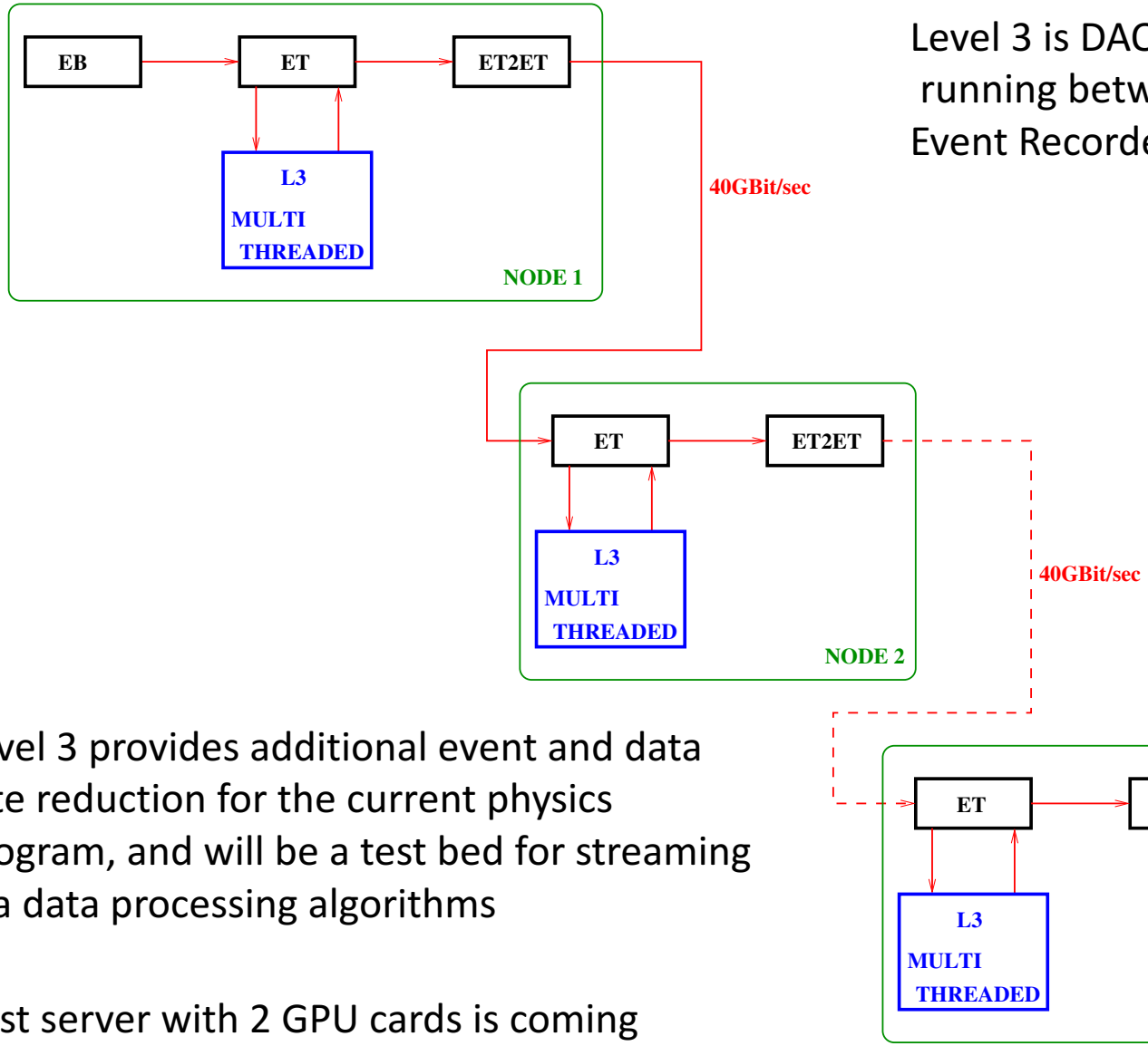


Existing fpga-based segment finder: hit-based, does not need timing calibration,
compares data with segment dictionary

Proposed segment finder: time-based, requires reasonable timing calibration,
fits data by straight line – suppose to improve segment position and angle resolution

Three basic operations: shift-and-sums, peak search in 2-dim array, and linear fit; will explore
fpga-, gpu- and cpu-based solutions

CLAS12 Level3 (software) trigger



Level 3 is DAQ component, running between Event Builder and Event Recorder, currently dummy

Level 3 provides additional event and data rate reduction for the current physics program, and will be a test bed for streaming era data processing algorithms

First server with 2 GPU cards is coming

Streaming Readout

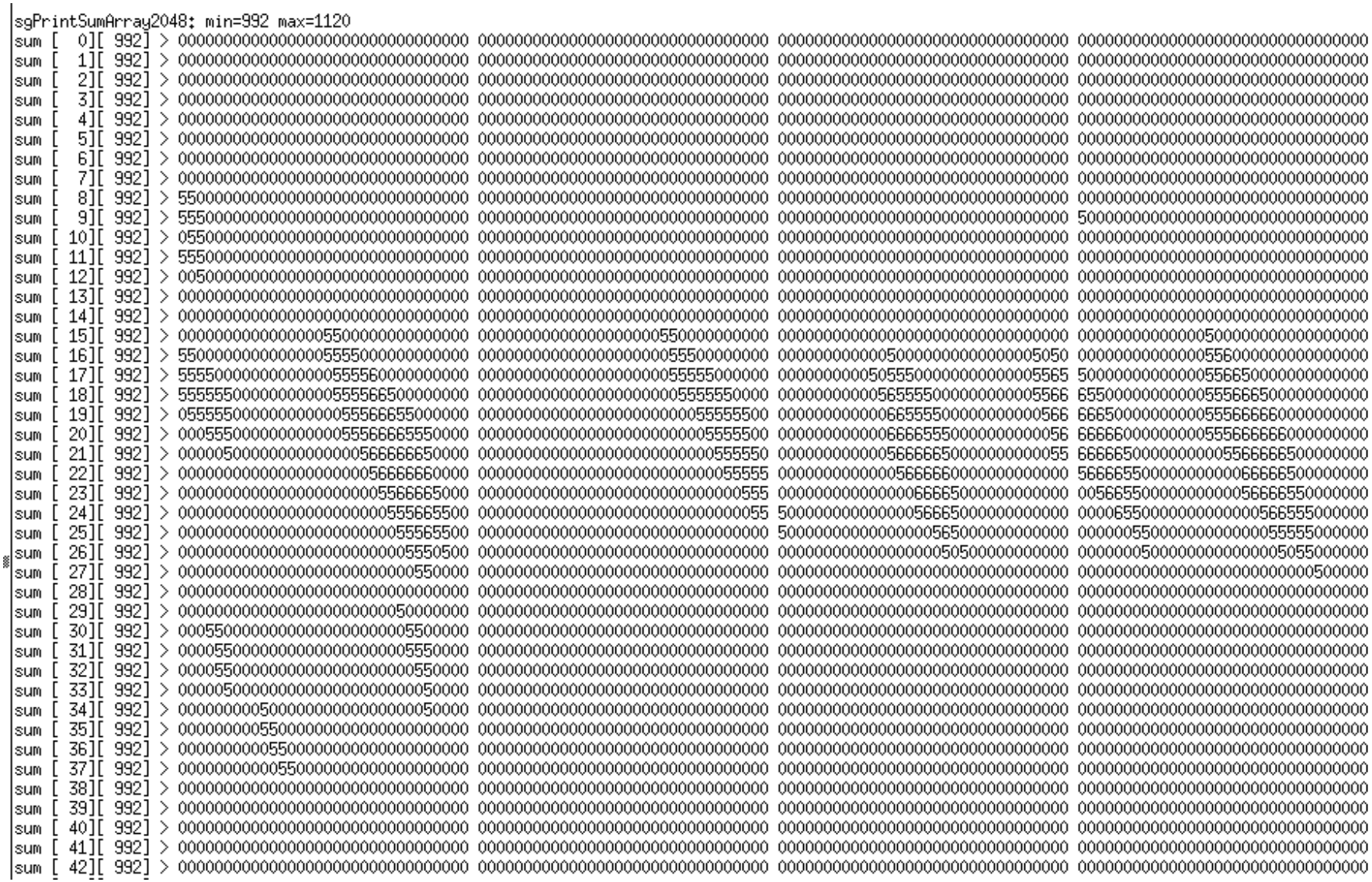
- In few years, CLAS12 front-end electronics should be ready for the streaming DAQ operation; back-end suppose to be developed by other groups
- CLAS12 is able to provide test beds for the streaming DAQ development, from relatively small setups (few VXS crates) up to 40-crate system where full scale streaming DAQ can be tested, with the data rate on the level of 50GByte/sec

Conclusion

- CLAS12 front-end upgrade plan is in progress, with the purpose to increase event rate up to 100kHz with existing triggered mode, and to make system compatible with streaming mode operation
- Data processing solutions for the future streaming operation will be developed and tested in frame of the new level3 trigger project for the current (triggered) operation
- We are working closely with jlab and outside groups assisting them with streaming DAQ back-end development

Supporting slides

Time-based segment finder: 2-dim peaks after shift-and-sum process



Segment angle

Segment position