ER2 Sensor Testing R&D

MIT (Automated) test system

Ivan Amos Calì 19/03/2024

MPI TS3500-ShieldEnvironment

300 mm Automated Probe System For accurate and reliable IV, CV, pulsed-IV, 1/f and RF and with WaferWallet® Option for Fully Automatic Measurements

FEATURES / BENEFITS

Designed for Variety of On-Wafer Applications
- Device Modeling - DC-IV, DC-CV, Pulse-IV, ESD, 1/f
- RF and mmW - RF Setup from 26 GHz to 110 GHz & beyond
- Wafer Level Reliability - for accurate stress- and measure conditions
- Drivers for leading test executive software suits

WaferWallet® Option
- Designed with five individual trays for manual, ergonomic loading of 150, 200, or 300 mm “modeling” wafers
- Fully-automated tests with up to five identical wafers at multiple temperatures
- Unique capability to load/unload wafers at any temperature

MPI ShielDEnvironment™ for Accurate Measurements
- Advanced EMI / RFI / Light-tight Shielding for best 1/f noise test results
- Ultra-low noise IV measurements down to fA level
- Programmable microscope movements for test automation and ease of use
- Wide temperature range -60 °C to 300 °C with unique configuration flexibility

Ergonomic Design and Options
- Easy wafer or single DUT loading from the front
- Integrated active vibration isolation
- Completely integrated prober control for faster, safer and convenient system and test operation
- The Safety Test Management (STM™) with automated dew point control
- Reduced footprint due to smart integration of the chiller
- Instrument shelf option for shorter RF cables providing the highest measurement dynamic

- Vendor product page with Data/Fact Sheets: https://www.mpi-corporation.com/ast/engineering-probe-systems/mpi-automated-systems/ts3500-series-with-waferwallet/
- CERN DAI: https://edh.cern.ch/Document/SupplyChain/DAI/10080285
- Main features:
  - Compatible with FormFactor CM300xi
  - RF environment up to 110 GHz
  - Automated test system ready
  - ShieldEnvironment
  - Very versatile software suite
  - Experience in using the wafer probe “in house”

Relevant features

Chuck, probe card, microscope

- 300 mm MPI ambient chuck high power / high voltage designed to work with thin wafers
- MPI probe card adapter 4.5 or 6 inches, 22 cm for round probe cards
    - Should be able to host any probe card
    - MPI provides a series of probe cards (also RF) designed in house: https://www.mpi-corporation.com/probecard/
    - At present we didn’t acquire any dedicated probe card as we were waiting to have more understanding of the needs
- Selected high resolution camera with several optics to have focal field from cm to um.

Extra features

Automatic loaders (non acquired but machine ready for it)

The WaferWallet®

Common practice for Device Characterization in the Modeling and New Technology Development processes is to extract data from a typical few wafers via extremely accurate IV-CV, 1/f, RF, mmW, and Load-pull measurements.

MPI's WaferWallet® extends the TS3500 series automation without compromising measurement capability. The WaferWallet® is designed with five individual trays for manual, ergonomic loading of 150, 200, or 300 mm "modeling" wafers. Fully-automated tests with up to five identical wafers at different temperatures are now possible.

The WaferWallet® MAX

MPI's WaferWallet® MAX is easy field upgradable to address the demand for faster time to market, collecting data from multiple 150 or 200 or 300 mm SEMI standard cassette.

Including advanced alignment technologies for pre-aligner and cassette scanner, optional top or bottom Wafer ID Reader and fully automatic exposure control, the WaferWallet® MAX is also available as an option for fully-automated measurements.

Relevant Features

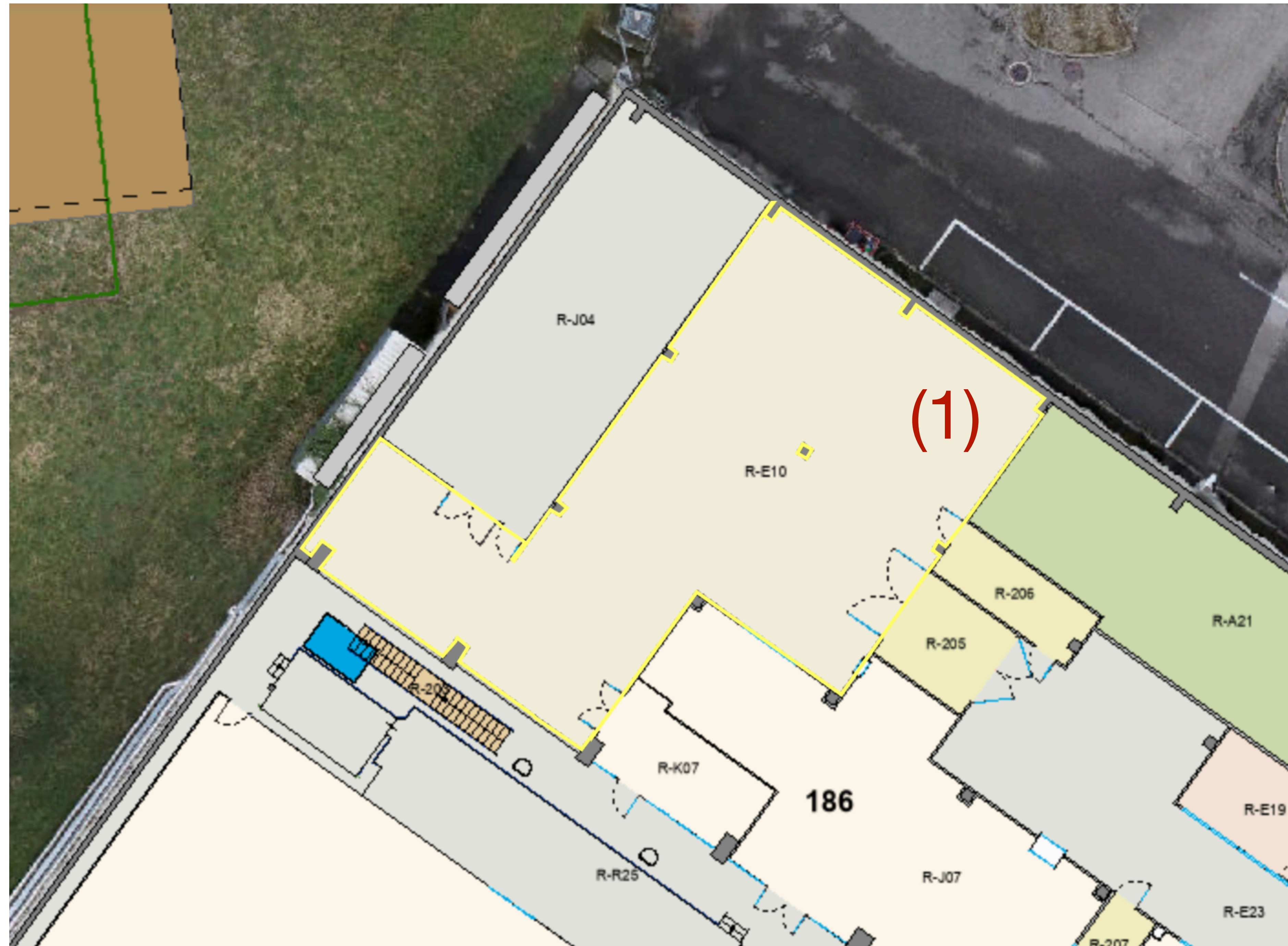
Software

- The wafer probe uses the SENTIO Software Suite
  - Quite modern and intuitive with very useful and dynamic features
  - RF application managed automatically by the software

- Emulator to run Velox Software included in the suite
  - CM300xi and MPI 3500 series are present in the SVT collaboration institutes and as far as we know there is full software compatibility
  - “In house” we have engineers willing to explore these features (iMAG Pro series)

Location

DSF



- It was decided to place the wafer probe in DSF in the CMS area (1)
- Big area available giving access to ITS3 and SVT collaborators
  - It allows collaborators of various institutes easily
  - At present the only activity planned for the wafer probe is the ER2/ER3 sensor test

MOSAIX testing: scenario A

Intro: during the test of the ALPIDE and ER1, it was considered/observed that the inductance and the resistivity added by a wafer probe test system were bringing the chip outside of the working parameters. Wire-bonded configuration was chosen for extensive test/characterization
→ **for ER2, this problem could be even more relevant since the 3 data links are at high frequency (10 Gbps)**
→ **not optimal contact on the power pads could induce jitter on the high-speed links**

Scenario A) "easy" but slow (same as for MOSS sensor)

- **On the wafer probe**: the wafer probe would be used only for basic functionality test and scan could be performed at 160 Mbps
- **Test card**: The characterization of the serializer and the high speed link could be done wire bonding a small fraction of the sensors to a test card.

→ this strategy would require multiple wafer probes, already for the ITS3

→ the high speed data transmission would be characterized only on a small fraction of the sensor prior to wire bonding

→ **very likely, it will not be realistic for the tests of the LAS**

MOSAIX testing: scenario B

Intro: during the test of the ALPIDE and ER1, it was considered/observed that the inductance and the resistivity added by a wafer probe test system were bringing the chip outside of the working parameters. Wire-bonded configuration was chosen for extensive test/characterization
→ **for ER2, this problem could be even more relevant since the 3 data links are at high frequency (10 Gbps)**
→ **not optimal contact on the power pads could induce jitter on the high-speed links**

Scenario B) Fast but with technical challenges

- Use the RF setup to perform full scans and high-speed link characterization directly on the wafer probe system

→ we think that this is the path we should follow and on which we should concentrate our efforts, and build a task force to design a high-frequency testing system with wafer probe

- we are discussing with MPI and with other probe-card vendor in order to evaluate the feasibility of this plan

- it will very likely require developing a dedicated probe-card system

- RF micro-manipulators/individual probes strategy should be evaluated as well

Wafer probe challenges

- In order to develop the testing strategy with wafer probe it has been decided to use the NKF7 serializer already produced during ER1 submission as a use case.

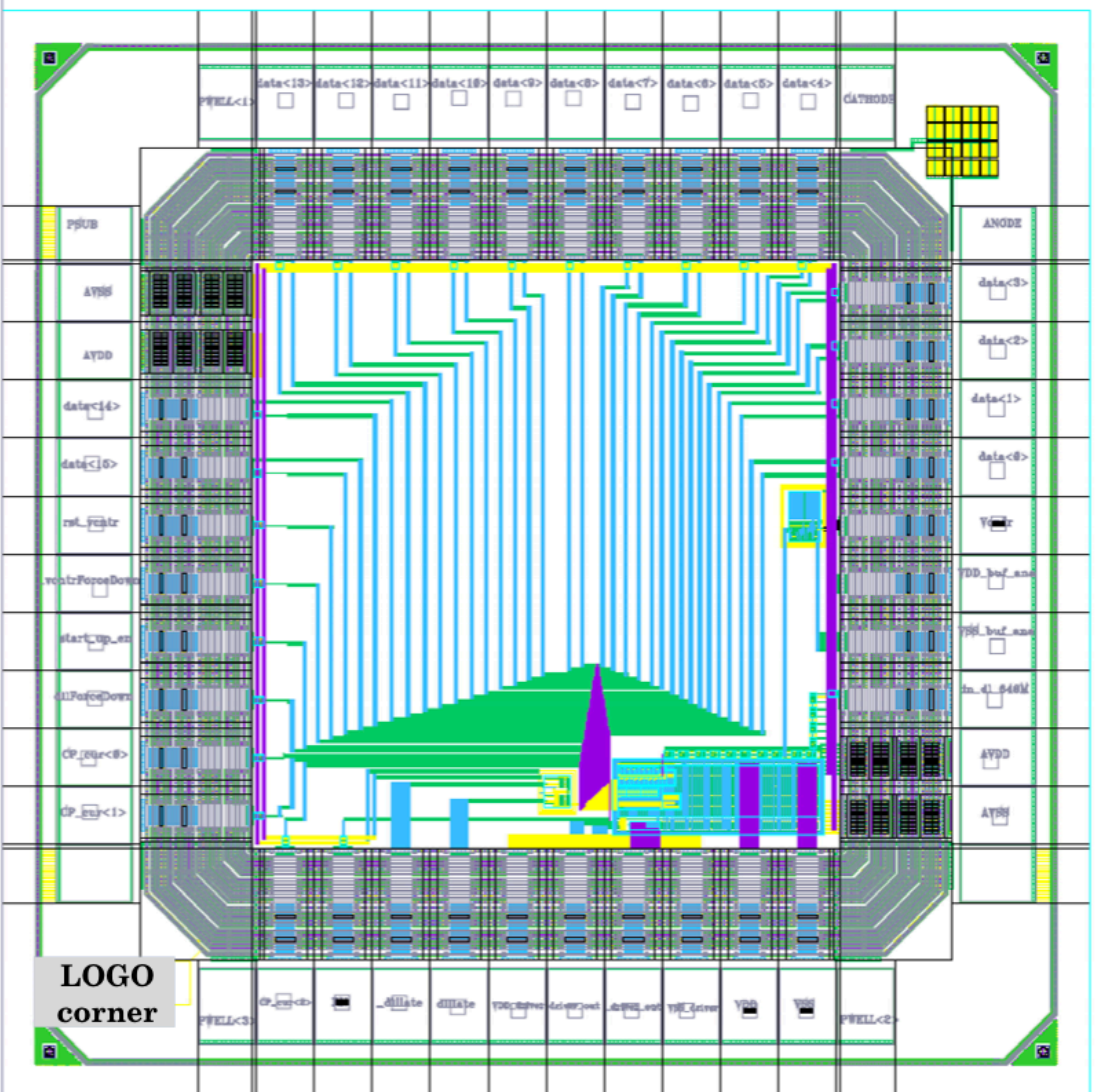
- The ASIC periphery is being designed by the Nikhef group and it is simulated for wire bonding connection
  - It is expected a wire-bond of 20 mohm and maximum length of 3 mm (numbers to be verified)
  - The feasibility studies about the possibility of using the wafer probe instead of wire bonding configuration is responsibility of the MIT team and the Korean team

- For MOSAIX is required the supply from both side of the sensor
  - If only one side supplied, the test should be done RSU by RSU instead of having the whole matrix operated at once

- At present the MIT team is in touch with the MPI designers to perform feasibility studies

NKF7 serializer

- Ref clk: 642 MHz , 16 bits input, output 10.27 Gbps



Digital Unit
Dual Port FIFO
DLL startup State Machine
PLL / DLL Lock Detectors
lock_dll_o
lock_pll_o
wdata_i
clk_w_i
rst_dp_i
en_su_dll_i
cfg_su_dll_i
rst_dll_i
en_dp_i
rst_pll_i
NKF6 PLL
NKF4-VCO
en_pll
RN
RN_vcntr
clk_ref
out_clk_320M
out_clock_640MHz
40MHz
NKF7
Analog Core
sdata_o
monitor_o<?:0>
in_dl_640
start_up_En ???
CP_cur<2:0>
NKF6 LDO
BGR
NKF1/2
VDD
VSS
res<7:0>
startup
Analog Unit

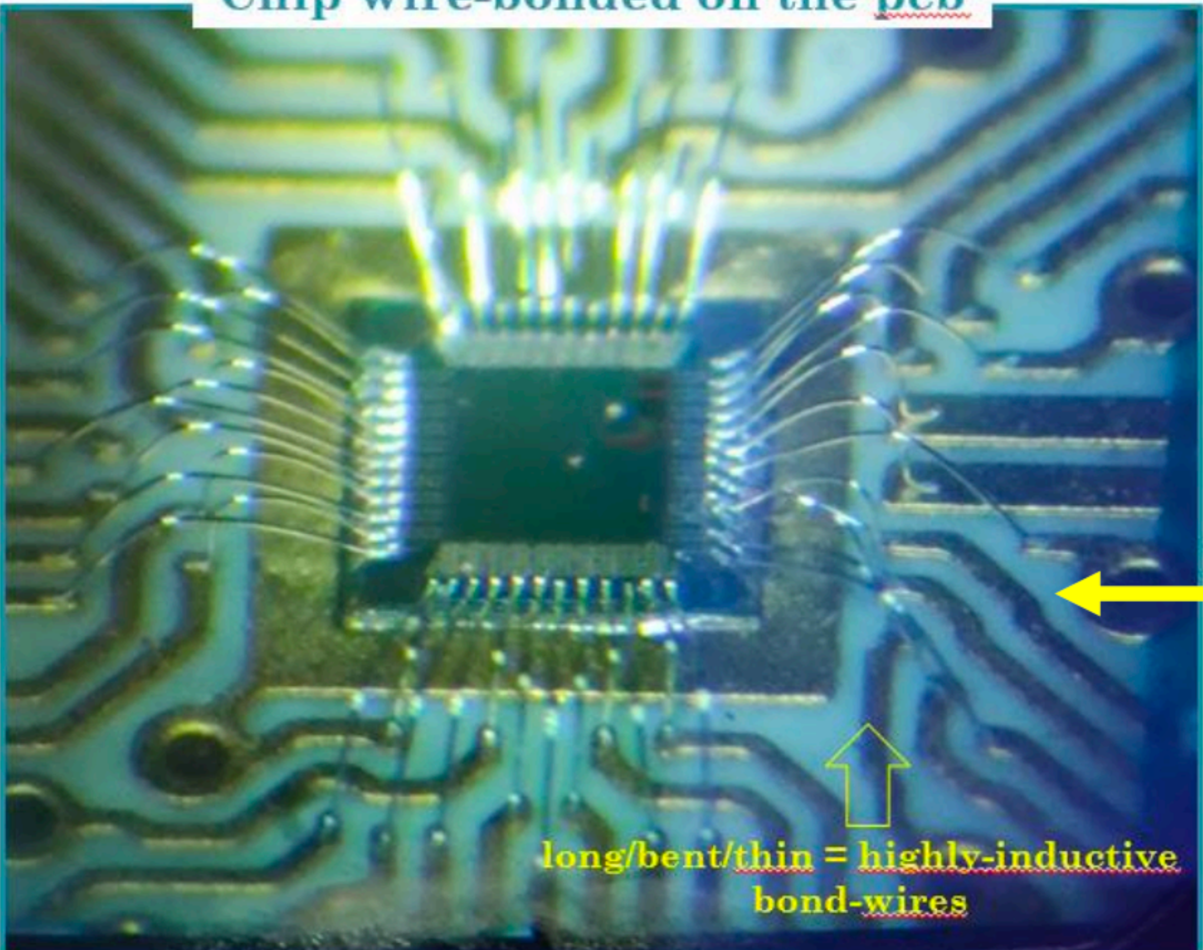
6-3-2024

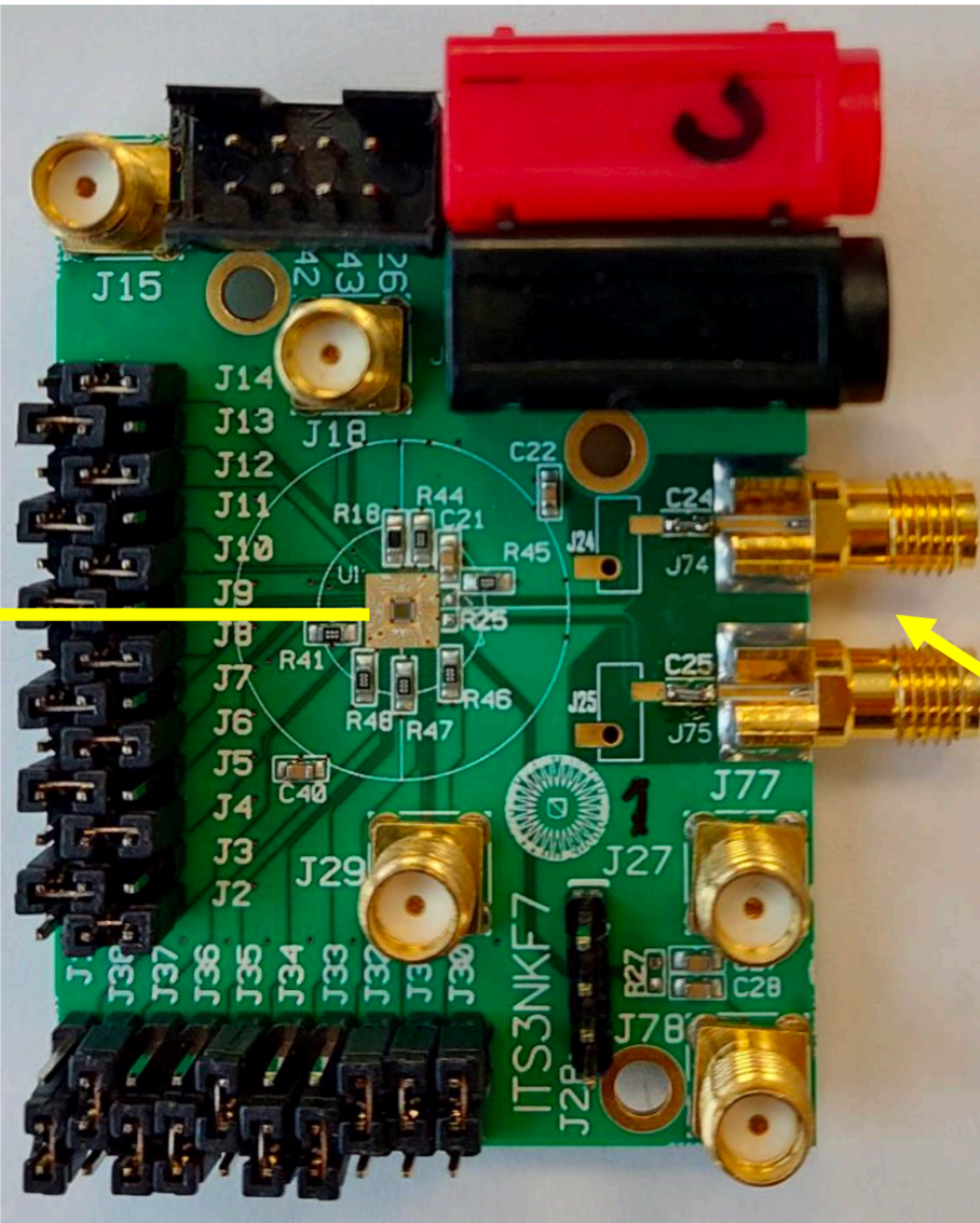
NKF7 serializer

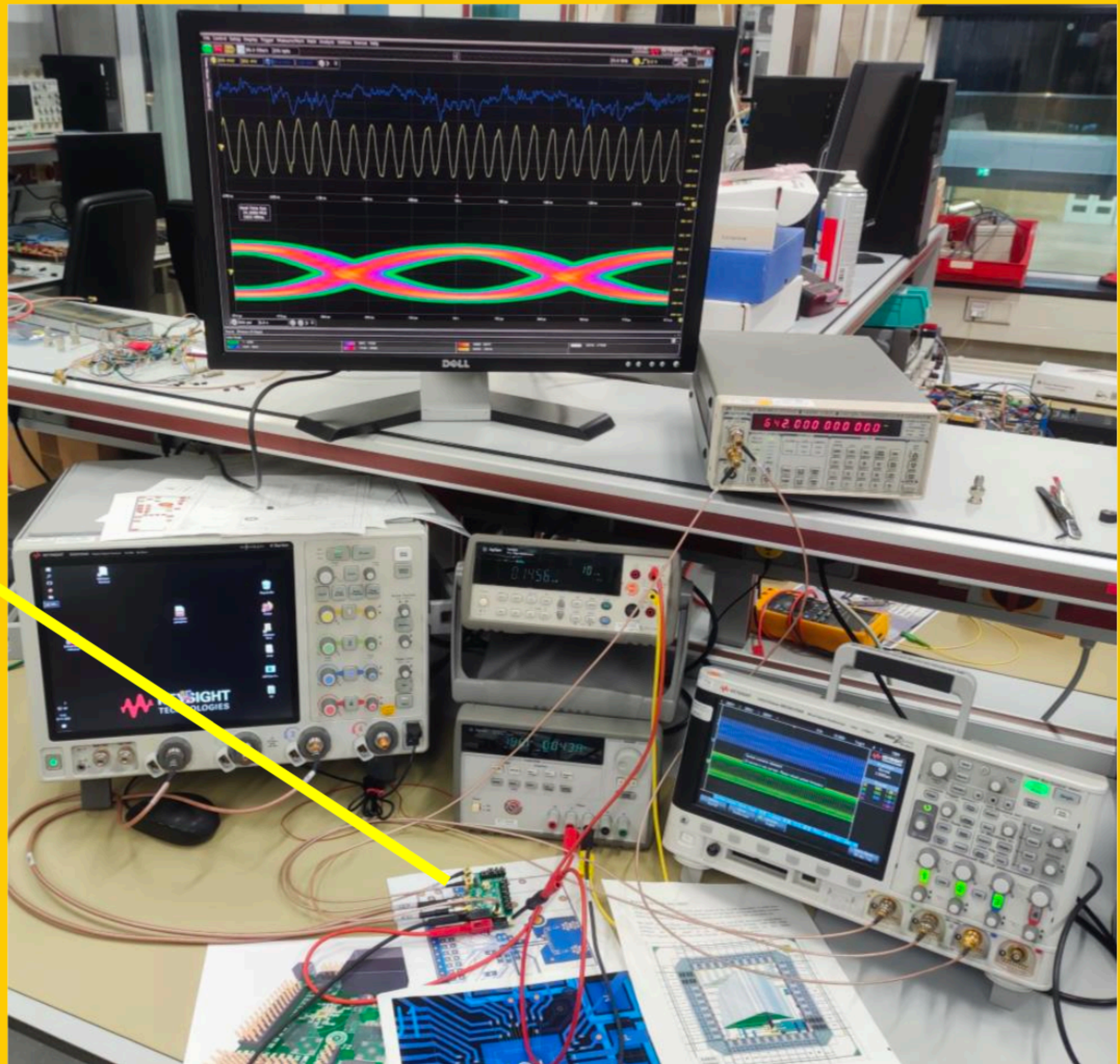
Full presentation: https://www.dropbox.com/scl/fo/v41zz5ib4ghk3xi9tsjrc/h?rlkey=32vxzrr5msu39nudo5n1khg0j&dl=0

Fixed pattern measurements

Carrier
- Edge mount SMA for high speed links
- Fixed pattern set by jumpers (v2 also has dipswitches)
- 4 layer board, Rogers material







First results reported last TWEPP
- Good output signals at 5Gbps
- At 10 Gbps some distortion
- Simulations suggest distortion from bondwire inductance

Self-generated power supply noise the Serializer test chip (NKF7)

lib: /icwork /vgromov/ALICE_ITS3/ITS3 cell: tb 167.sch DUT: GWT PSI TOP_4_VG_verif_2, lib:ITS3, view: schematic, simulation : tt, +25C,

Test bench

data rate =10Gbps, pattern : 010101, VDD_ext = 1.2V

$L_{bondwire}$ = 0 nH

$L_{bondwire}$ = 2 nH

$L_{bondwire}$ = 5 nH

- the internal current switching activity in the Serializer circuit will cause the distortions (noise) generation on the power supply voltage as a result of the voltage drop on the bondwire inductances
- the effect gets less pronounced at the lower values of the bondwire inductances (<2nHn)

Output differential signals assymetry / distortion effect

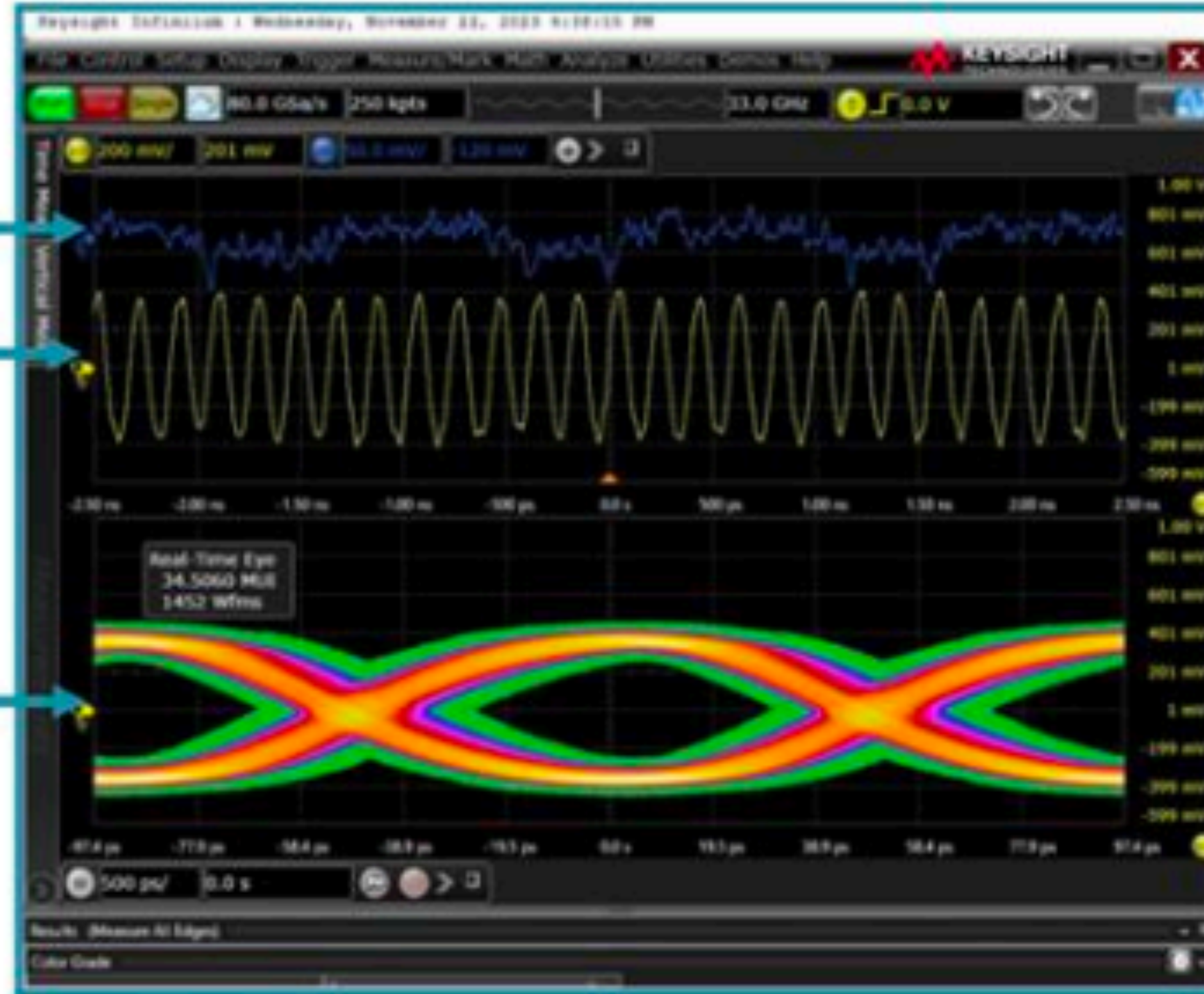
Operation at 10.27Gbps, 16-bit data pattern : 0101010..., F_clock_ref_DLL = 642MHz , chip2(black)

CM signal: (Vout_p + Vout_n) / 2

Diff signal: Vout_p - Vout_n

Eye Diagram @ Diff signal

VDD_driver = VDD (core) = 1.366V



VDD_driver = VDD (core) = 1.2V

VDD_driver = VDD (core) = 1.15V

- the output signals assymetry (distortions) are periodic and synchronous to a 16-bit data pattern (reference clock period)
- **the effect is less pronounced at higher power supply voltages (1.366V)**
- it looks like the transistors are not fast enough to cope with the required switching speed causing the distortions at 10Gbps

Summary NKF6 PLL:

Enable PLL startup screenshot looks ok:

- **Last bit longer 4μs i.s.o. 2μs=>ok for now**
- **Locked active before Vctrl stabilized => ok for now**

f_o vs f_i looks ok:

- **Fit shows $f_o = 16 * f_i$**
- **UU and Nikhef measurements show similar results for f_o vs V_{ctrl}**

Jitter measurements are concerning:

- Measured 80 ps_{pk-pk} i.e. 3 times larger than specified ($35ps_{pk-pk}$)
- Spectrum measurement shows some structural (non gaussian) origin
- Measuring jitter in output period with fixed relation input clock, jitter drops to 10 ps_{pk-pk}
- Measurement indicate that output clock period depends on position in input clock period. Maybe some GND/VDD bounce effect or Xtalk related to the input clock
- Jitter fade out pattern similar with different input clock frequencies (31.3-40-46 MHz)
- Jitter reduces (23-19ps and also in spectrum) after adding 100 nF capacitor

Summary NKF6 PLL:

- Observed remarkable correspondence between VDD_VCO distortion measured at Nikhef and the periods of each of the 16 cycles measured at Utrecht University
- At Utrecht NKF4-VCO characterization showed that distortion on VDD_VCO are FM modulated on the output with 3mV/MHz sensitivity. The VDD_VCO series resistor distortion of 70mV (at 50Ω) then should give 56 ps_{pk_pk} jitter. Placing capacitor (which eliminates the series resistor distortion) reduces jitter from 85 to 70 ps_{pk_pk}. So then the series resistor is responsible for $\sqrt{(85^2-70^2)}=50$ ps_{pk_pk} which is close to the calculated jitter of 56 ps_{pk_pk}

Summary

- MIT is being equipped to perform tests and characterization of the ALICE ITS3 ER2/3 and the SVT sensors
  - A wafer probe complete test strategy is being developed
  - Involvement/extension in the design of the already existing test system
- MIT is also involved in the sensors readout chain and SVT readout.

Backups

Preliminary MPI answer

1. For MPI vertical probe card, 50 probes and 10Gbps is no issue, as long as the device pitch over 40um.

2. If customer's device is combining RF and high speed DC Test, then we can only support AST RF module plus MPI High speed CPC, max up to 6Gbps.

3. The probe card overall path resistance from PCB, substrate to probe tip, we can control within 5 ohm, depends on how large the PCB size is. However between channel to channel resistance difference, we can control within 1~2 ohm.

Preface and disclaimers

- Following up discussion initiated at the beginning of 2023 MIT decided to consider the purchase of wafer probe that should be compatible with the needs of the SVT and ITS3 project. The specs used for the purchase were the one known at the beginning of 2023

- Considering what present already at CERN and in other institutes collaborating with MIT, MPI and FormFactor were asked for offers and the full acquisition process (including demonstrations) was developed in close contact with Jerome A. as expert of wafer probes

- In these slides it is presented what is being acquired as a core system but MIT is willing to consider extending the accessories and features list as per specs of the ER2/ITS3/SVT test system.

Extra features

Microscope

	iMAG-M	iMAG	iMAG Pro	iMAG-II	iMAG-II Pro
	iMAG®-M The Digital Microscope	iMAG® The Digital Microscope	iMAG® The Digital Microscope	iMAG® II The Digital Microscope	iMAG® II The Digital Microscope
Max. video resolution	6.55 MP color			12 MP color	
Max. video speed	20 fps real color frame rate				
Max. picture resolution	2560 x 2560 pixel			4024 x 3036 pixel	
Max. lens Z drive range*	N/A	N/A	4 mm	N/A	4 mm
Automatic lens detection	N/A	Yes			
Lens compatibility	With any M Plan lenses				

**Depends on system's type and configuration*

Optical Specification

Objective Lens[1]	Optical Resolution[2] [µm]	N.A.	Working Distance [mm]	Depth of Focus[1] [± µm]	Max. FOV [µm][3]	
					H	V
2x	5.0	0.055	34	90.91	9850	9850
5x LWD	2.0	0.13	45	14.03	3940	3940
5x	2.0	0.14	34	14.03	3940	3940
10x	1.0	0.28	33.5	3.51	1970	1970
20x	0.7	0.42	20	1.56	980	980

(1) 5x lens is part of standard delivery
(2) Optical resolution and focal depth based on reference wavelength of 550 nm. The optical resolution is identical over the entire FOV (!)
(3) Max. FOV is valid for all iMAG Series

- iMAG Pro was selected with extra lenses for few um resolution