Sensor design Update

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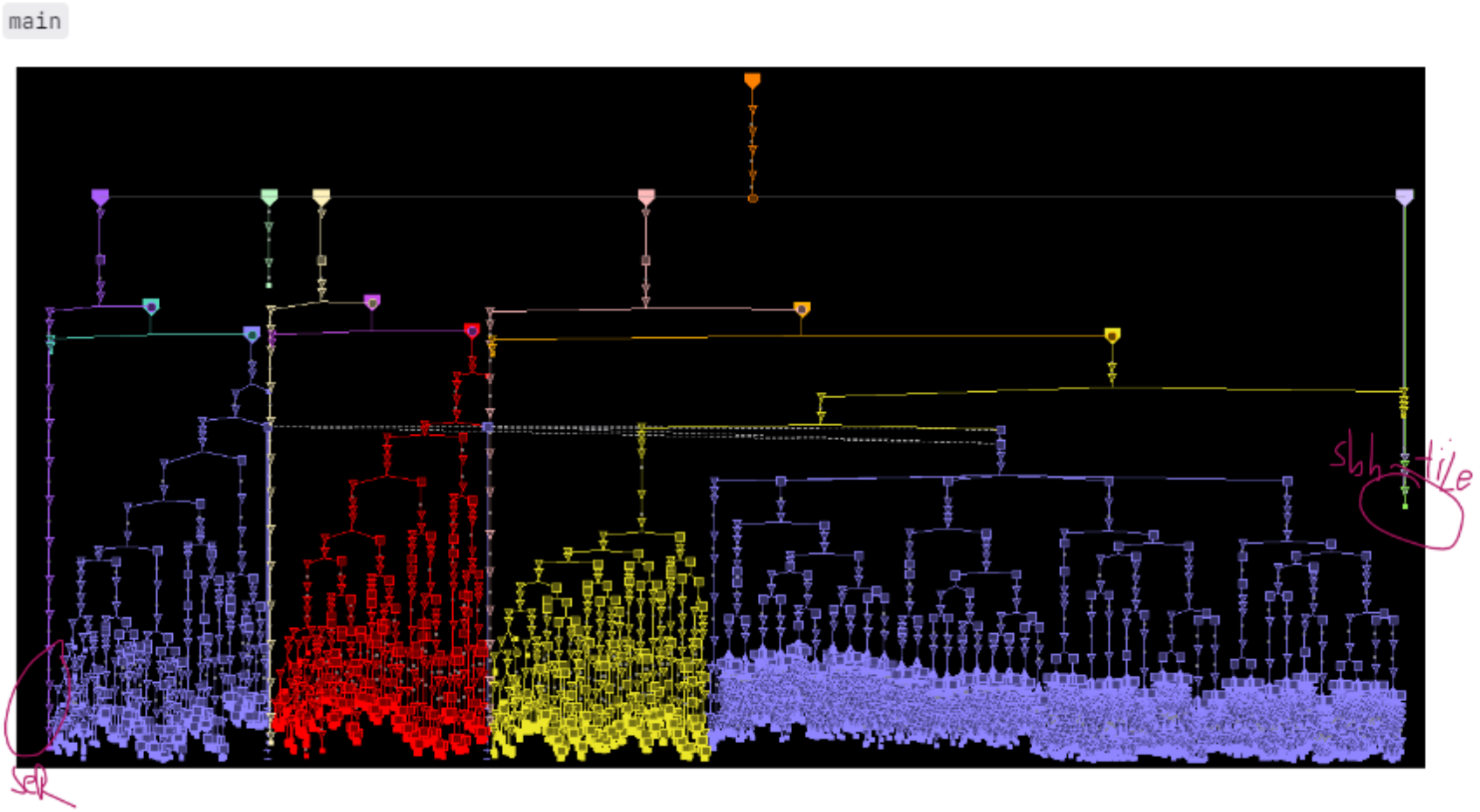
Timing issue in the periphery



https://gitlab.cern.ch/mosaix/mosaix_rtl/-/merge_requests/691

Setup and hold violations

```
#############################################################
Path 1: VIOLATED (-3.330 ns) Setup Check with Pin sbb_tile_wrapper_inst/sbb_tile_inst/sbb_clk_i->ser_data_a_i
          View: av_normal_max_rcworst_setup
         Group: clk_ser
    Startpoint: (R) serializer_inst/load_rdataA_reg[3]/CK
         Clock: (R) clk_160MserA
      Endpoint: (F) sbb_tile_wrapper_inst/sbb_tile_inst/ser_data_a_i
         Clock: (F) clk_ser

                  Capture       Launch
  Clock Edge:+     3.000        0.000
 Src Latency:+    -6.33 7      -3.635
 Net Latency:+     1.330 (P)    4.097 (P)
     Arrival:=    -2.007        0.462

       Setup:-     0.349
 Uncertainty:-     0.300
 Cppr Adjust:+     0.093
Required Time:=    -2.564
 Launch Clock:=     0.462
    Data Path:+     0.304
       Slack:=    -3.330
Timing Path:
```

```
#############################################################
Path 1: VIOLATED (-3.576 ns) Early Output Delay Assertion
          View: av_normal_skew2_rcbest_hold
         Group: clk_160MserC
    Startpoint: (R) sbb_clk_i
         Clock: (R) clk_ser
      Endpoint: (F) sbb_tx_data_p_o
         Clock: (R) clk_160MserC

                  Capture       Launch
  Clock Edge:+     0.000        0.000
 Src Latency:+    -5.791       -5.791
 Net Latency:+     5.944 (P)    0.000 (I)
     Arrival:=     0.153       -5.791

 Output Delay:-     0.100
  Uncertainty:+     0.050
  Cppr Adjust:-     0.000
Required Time:=     0.103
 Launch Clock:=    -5.791
    Data Path:+     2.318
       Slack:=    -3.576

#-------------------------------------------------------------------------------------------------------------------------------------
# Timing Point                                  Flags  Arc                    Edge  Cell          Fanout  Trans   Delay  Arrival
#                                                                                                        (ns)    (ns)     (ns)
#-------------------------------------------------------------------------------------------------------------------------------------
  sbb_clk_i                                    -      sbb_clk_i              R     (arrival)          1  0.750   0.216   -5.575
  CTS_ccl_inv_01882/Y                           C1C2  A->Y                   F     DFMCLKINVD8        1  0.750   0.167   -5.408
  CTS_ccl_inv_01881/Y                           C1C2  A->Y                   R     DFMCLKINVD8        1  0.093   0.153   -5.256
  CTS_ccl_inv_01880/Y                           C1C2  A->Y                   F     DFMCLKINVD8        1  0.077   0.166   -5.089
  CTS_ccl_a_inv_01879/Y                         C1C2  A->Y                   R     DFMCLKINVD16A      1  0.094   0.140   -4.950
  sbb_tile_wrapper_inst/sbb_tile_inst/sbb_data_p_o  -      sbb_clk_i->sbb_data_p_o  F     sbb_tile           1  0.149   1.299   -3.651
  CTS_ccl_inv_00727/Y                           C1C2  A->Y                   R     DFMCLKINVD4        1  0.130   0.090   -3.561
  CTS_ccl_a_inv_00003/Y                         C1C2  A->Y                   F     DFMCLKINVD4        1  0.038   0.088   -3.473
  sbb_tx_data_p_o                              -      sbb_tx_data_p_o        F     -                  1  0.066   0.000   -3.473
#-------------------------------------------------------------------------------------------------------------------------------------
    Other End Path:
```