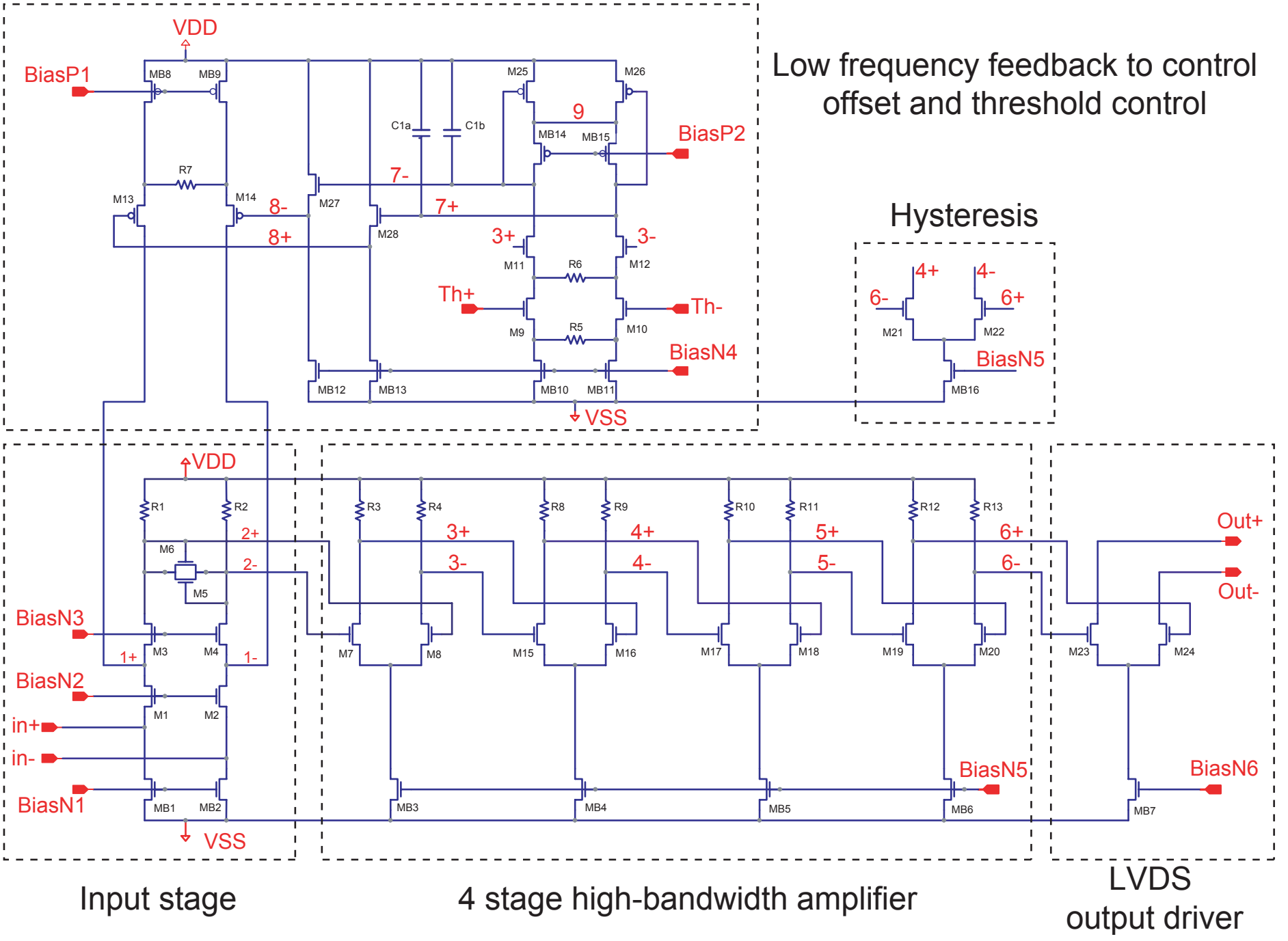
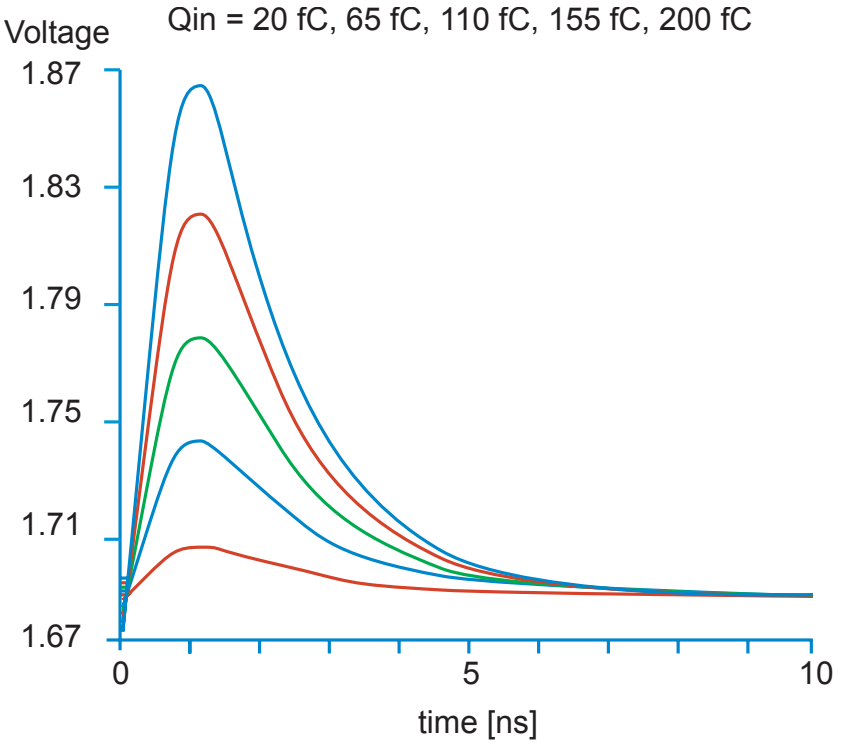
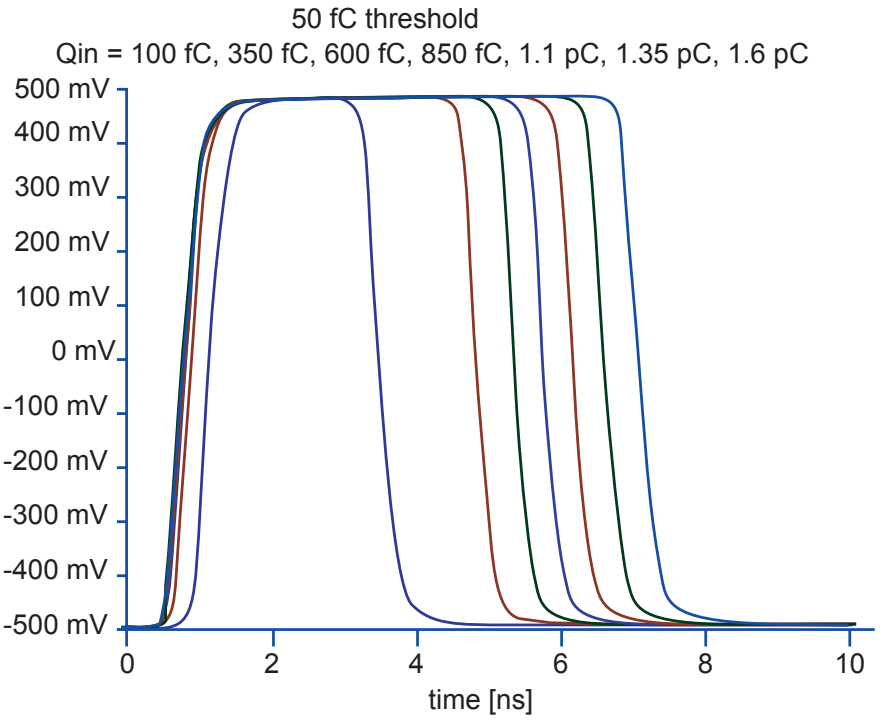
The NINO-ASIC (CERN, differential 8-channel comparator)



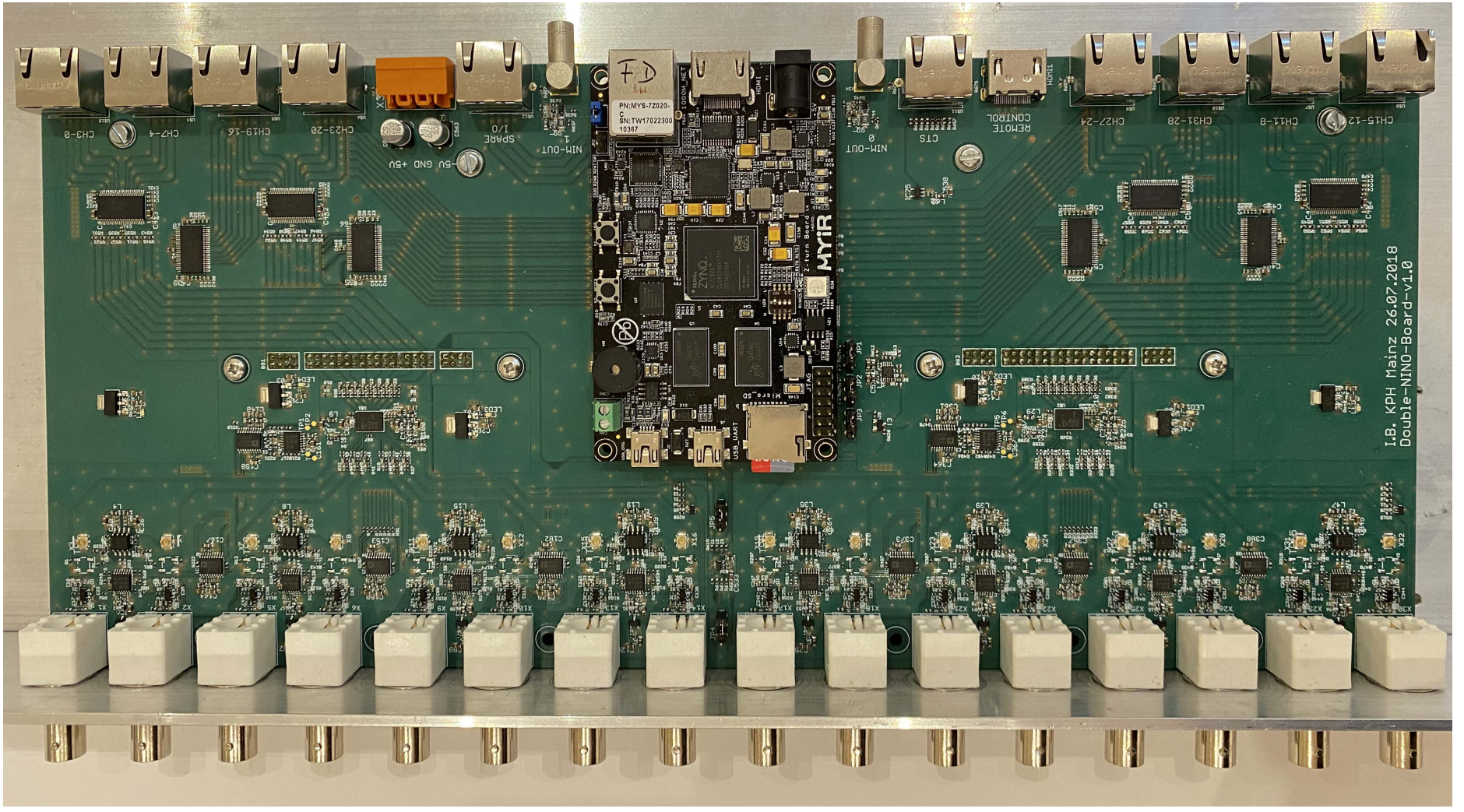
Pulse-Height: Time-over-Threshold





- Measure Time-over-Threshold
- Same pulse shape $\rightarrow$ function of pulse height
- Required: TDC with rising and falling edge

KPH NINO-Board

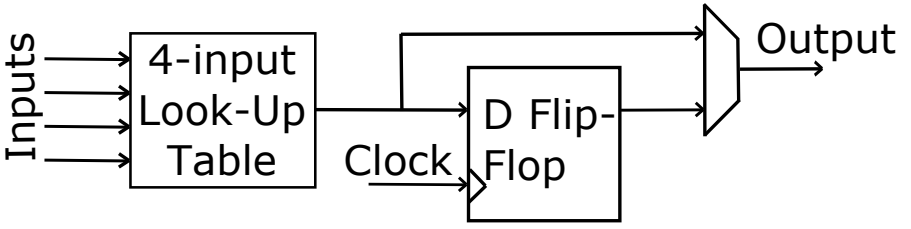


- 32 Channels to 4 NINO
- Individual input attenuators
- Input to Z-Turn ZYNQ, 2 NIM out, 2 spare LVDS in/out, 32 LVDS Channel out

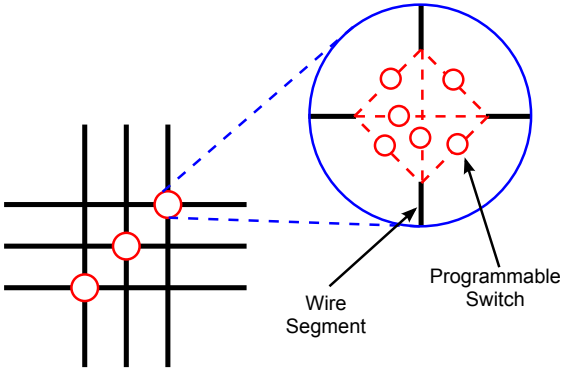
Reminder: What is a FPGA?

Field Programmable Gate Array

- Matrix of elementary building blocks, called “SLICE”:



- Programable connections

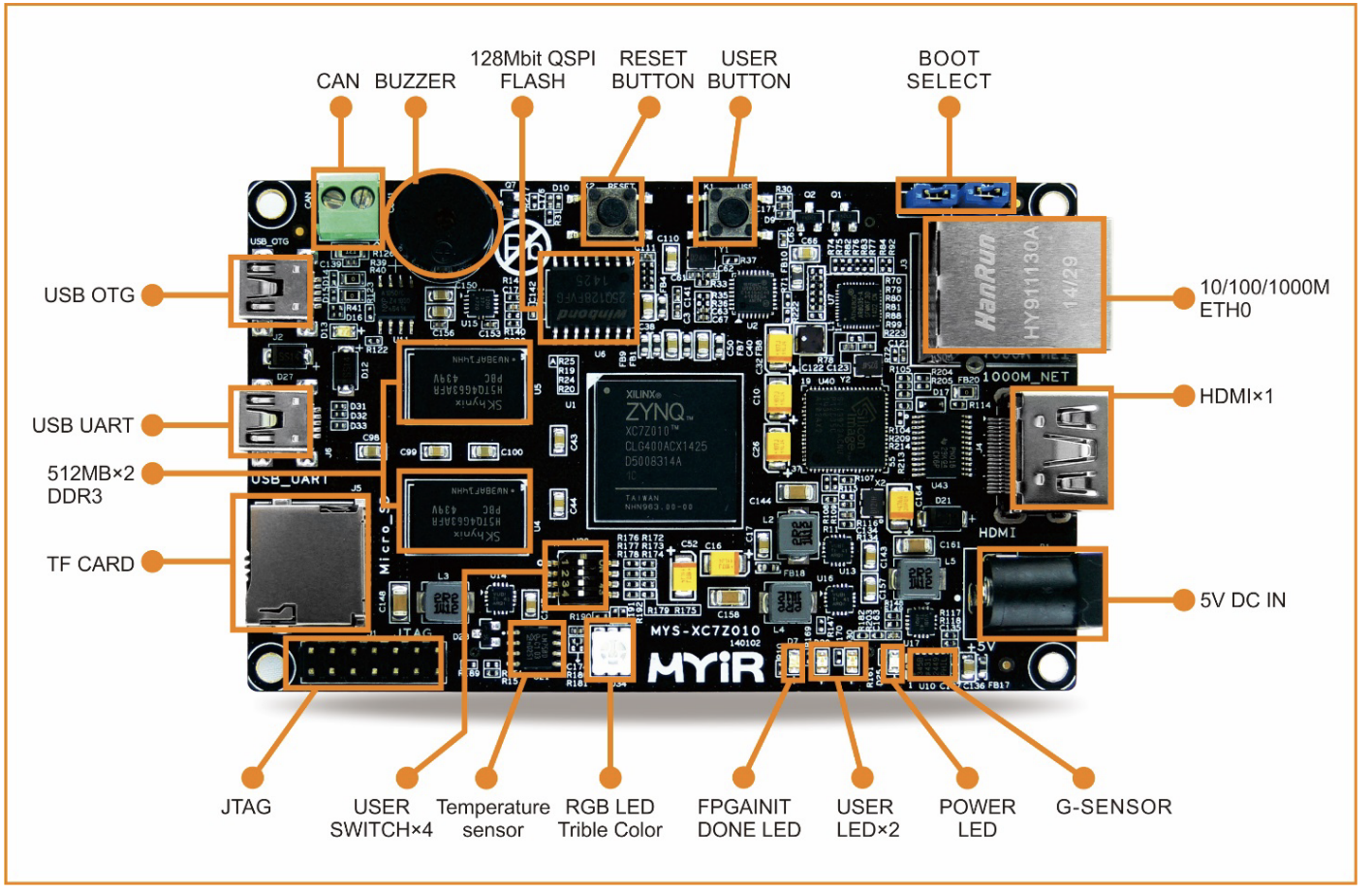


- Periphery
  - Clock generation via Phase-Locked-Loops (PLL)
  - I/O-Blocks (a lot!)
  - Block-RAM as medium sized memory blocks
  - Special elements, e.g. Digitial Signal Processing blocks

System-on-a-Chip (SoC)

Combined on a SINGLE Chip (e.g. Xilinx ZYNQ XC7Z020):

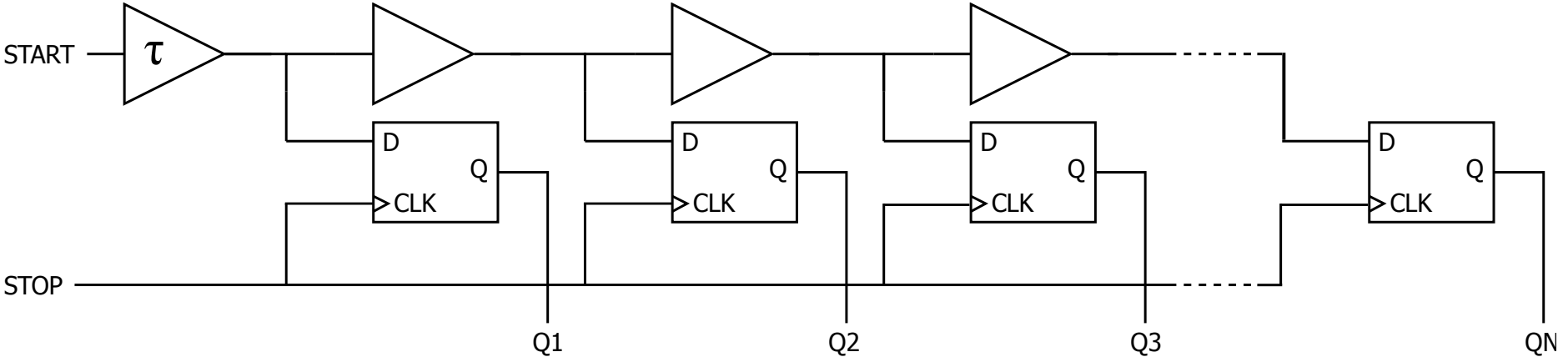
- ARM A9 866MHz Dual-Core Processor
- Artix-7 FPGA: 85000 Logic-Cells, 53200 Look-up-Tables, 106400 FlipFlops



MYiR, Z-Turn Board: $\approx 150\,€$, 1 GByte DDR-Ram, Ethernet, SD-Card, USB

Building a TDC on a FPGA (Based on code of Delft-University)

- Classical: Start - Stop $\Rightarrow$ Time difference
- Now: Clock (here: 250 MHz) $\rightarrow$ Binary counter gives *absolute* time
- Latch of counter with input signal $\Rightarrow$ **Coarse Time**, 4 ns resolution
- **Fine Time** with *Delay-Line*



with clock signal latch of delay time

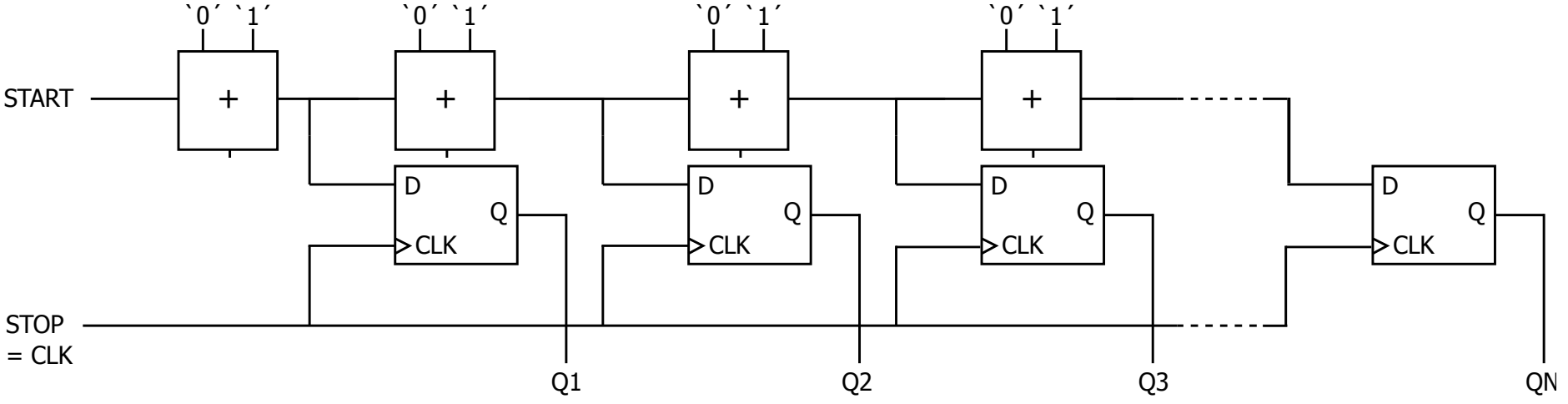
Efficient implementation of Delay-Line: Carry Chain

- Frequent addition of binary numbers (e.g. counters) $\Rightarrow$ FPGA is optimized for this!
- Example:

$$\begin{array}{rl} & 11111111111111111111111111111111 \\ + & 1 \\ \hline = & 10000000000000000000000000000000 \end{array}$$

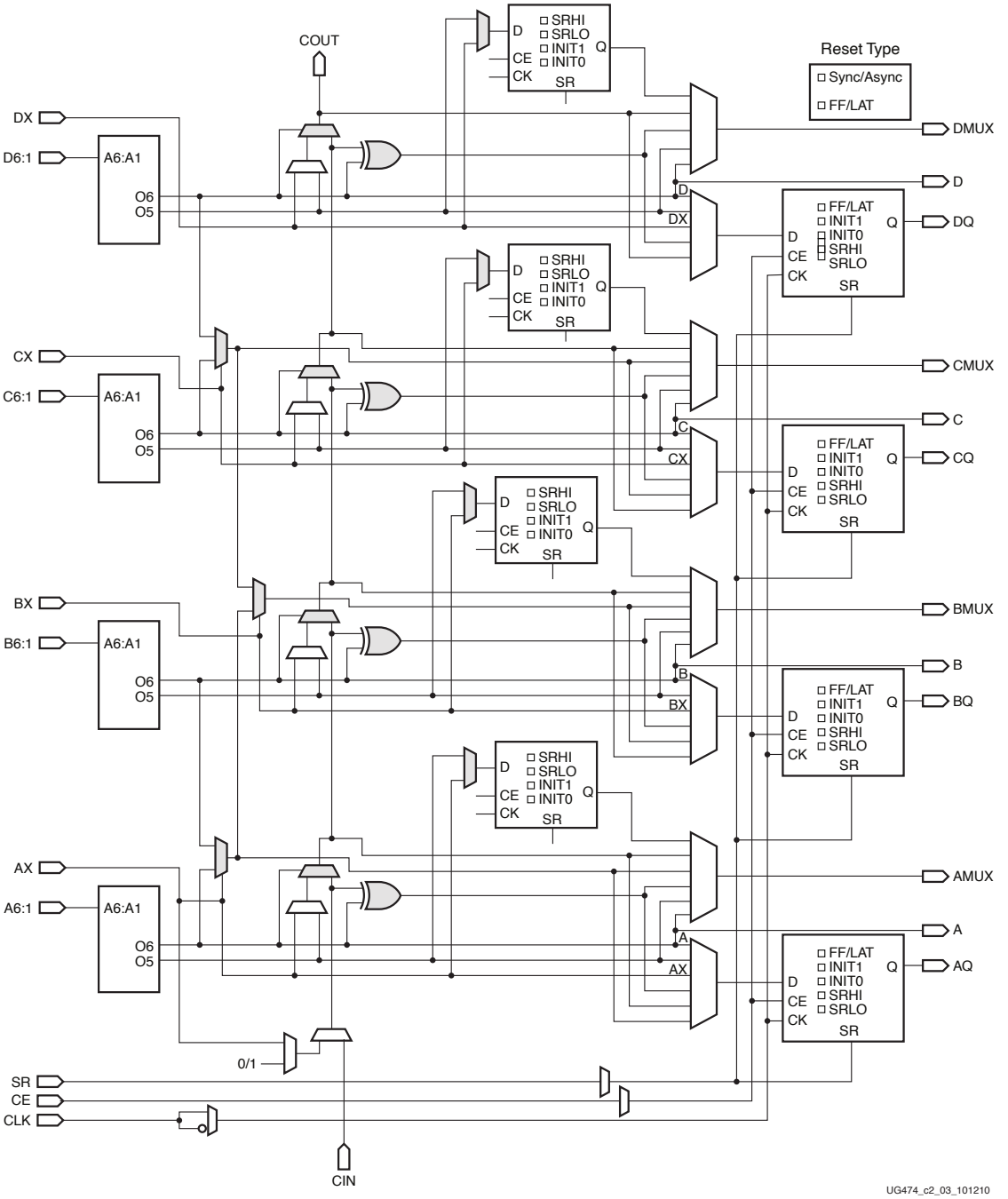
  Carry-Bit runs over complete word width

- Start with Input Signal, Stop on clock cycle:



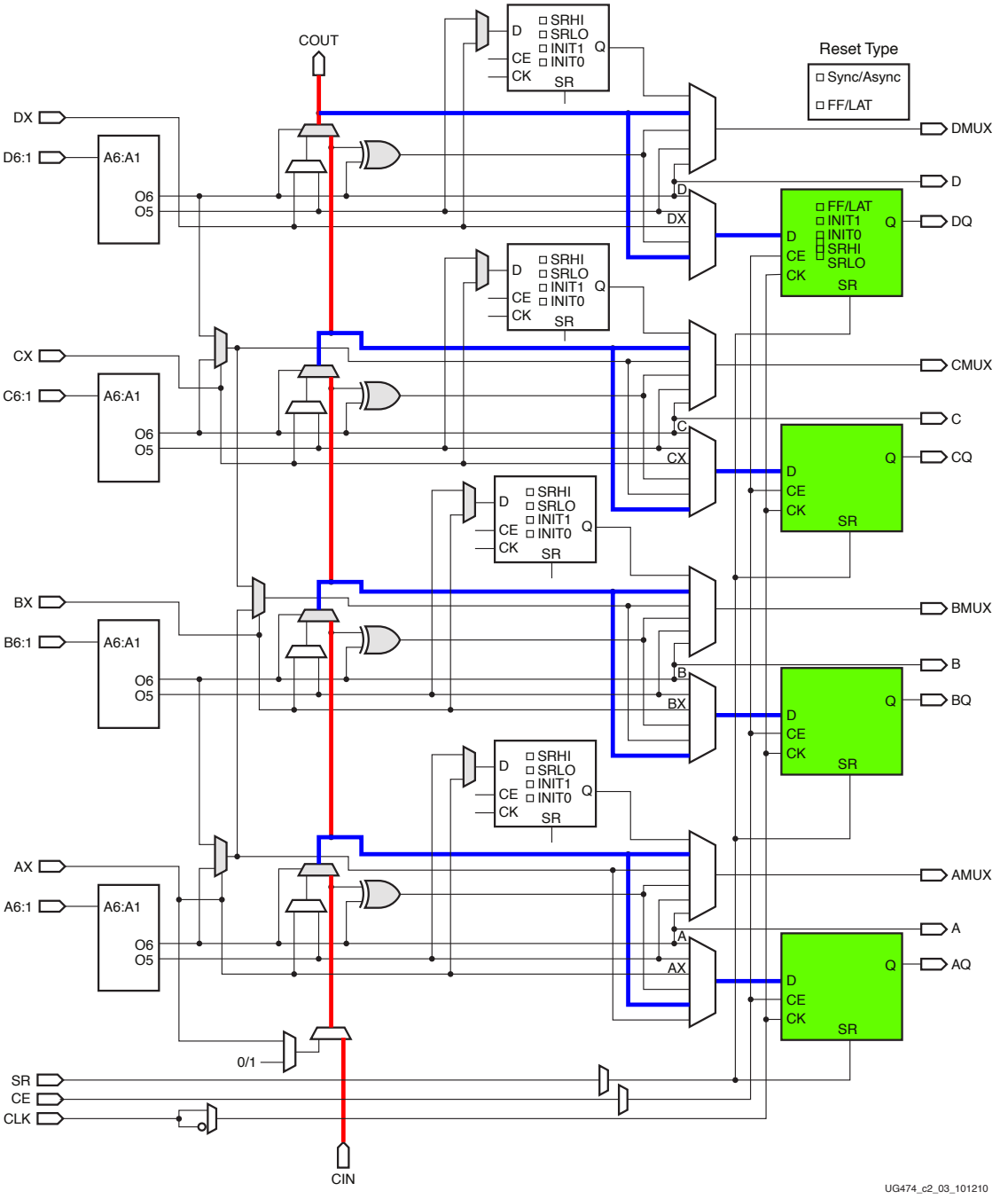
- ZYNQ: ≈ 18 ps per Carry-Bit $\Rightarrow$ 256 Bit length of delay line

Xilinx Artix-7 Slice

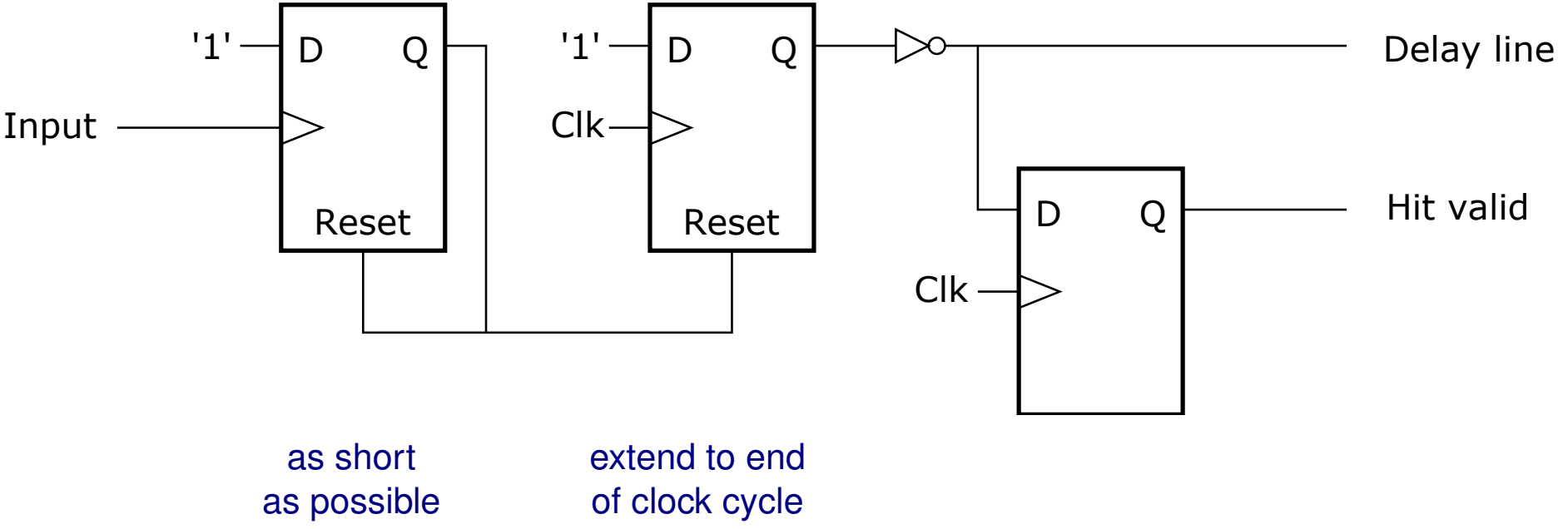


4× 6-2-Look-up 4-Bit CARRY 8× Flip-Flop

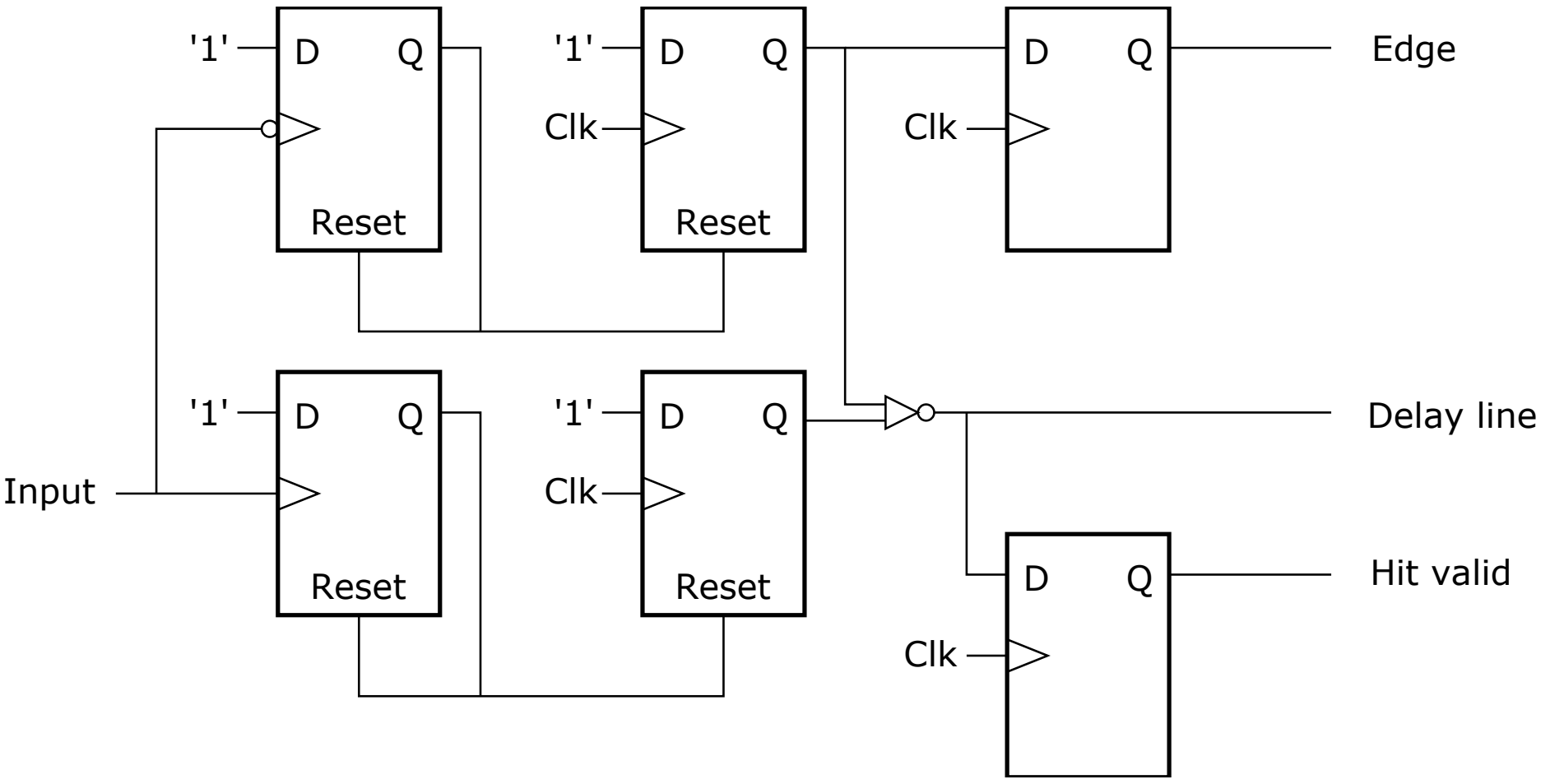
Xilinx Artix-7 Slice



Input stage


'1'
D
Q
Input
Reset
'1'
D
Q
Clk
Reset
Delay line
D
Q
Hit valid
Clk
as short
as possible
extend to end
of clock cycle

Input stage with rising/falling edge



Last step: Thermometer Decoder

Convert Bit-“Thermometer” to binary:

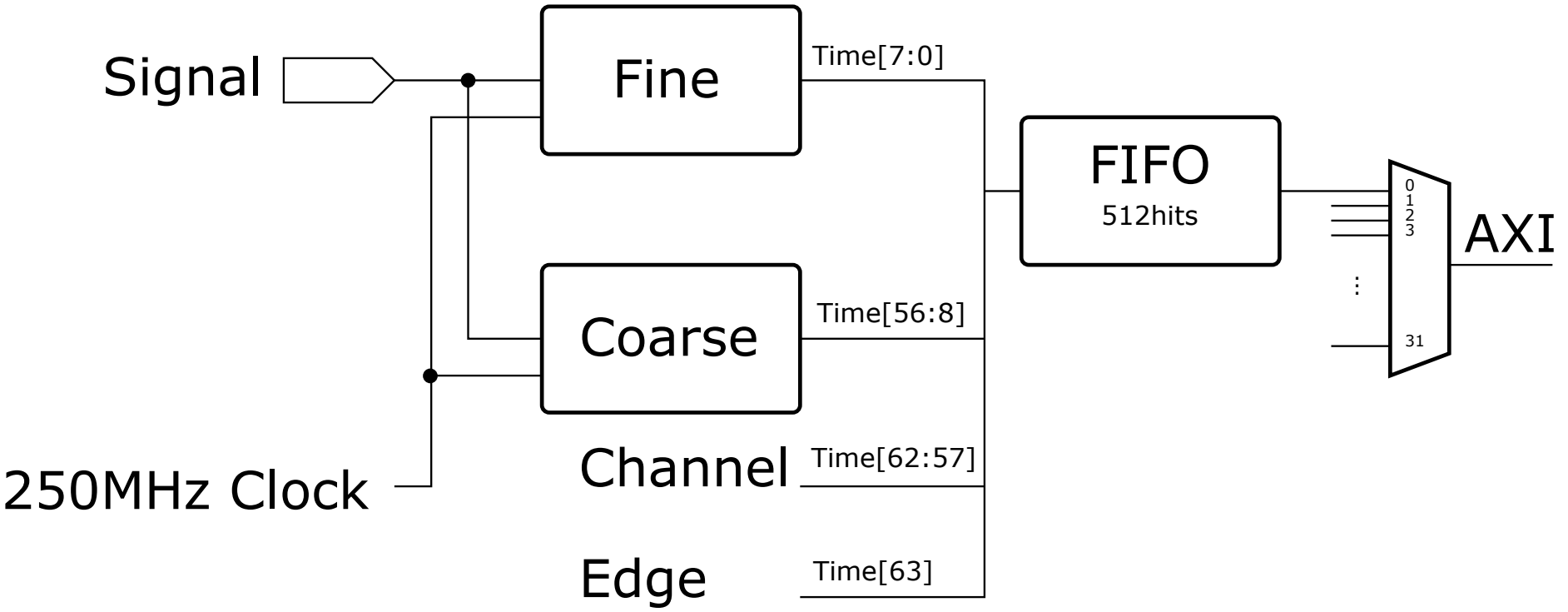
$$000000000000\underbrace{1111111111111111}_{n \text{ bits}} \quad \Rightarrow \quad \underbrace{00010011}_{n \text{ in binary}}$$

Possible strategies:

- Direct decoding with multiplexer logic (fastest, problem: “Bubbles”)
- Counting ’1’ bits
- Detected only highest ’1’ bit

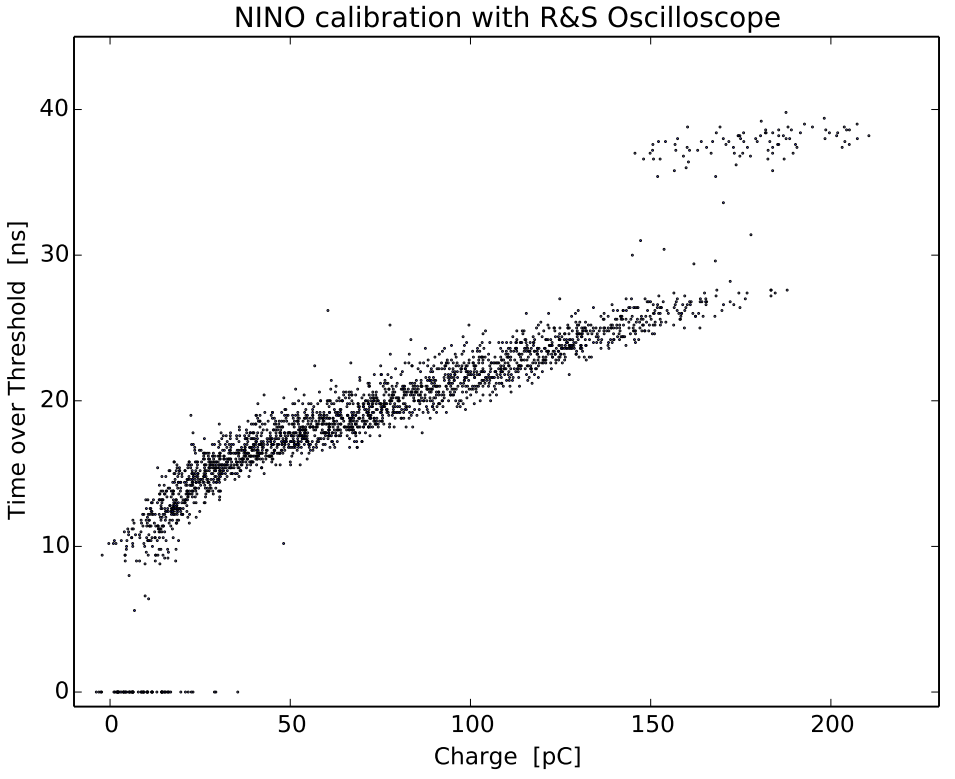
at the moment: multiplexer logic for lower part, counting top 16 bits

Block LAYOUT



- Buffer hits in “First In - First Out” Register (Block RAM)
- Dead time: 1 clock cycle ⇒ 4 ns ⇒ max. 250 MSamples/s (Burst)
- **asynchronous** read by CPU ⇒ mean rate given by network
  (≈ 30 MHz bei 1000MBit/s)
- **BUT:** CPU can select trigger window!

Summary



NINO-Board with FPGA TDC

- At the moment: 32 channels
- Resolution (RMS): 50 ps, might be improved (hard limit: 20ps)
- High rates (250 MSamples/s)
- Bursts are buffered per channel on fabric
- Complex Trigger on FPGA fabric possible
- SoC (complete Linux): Flexible Trigger programming, EPICS, NTP, High level debugging, etc.