Update

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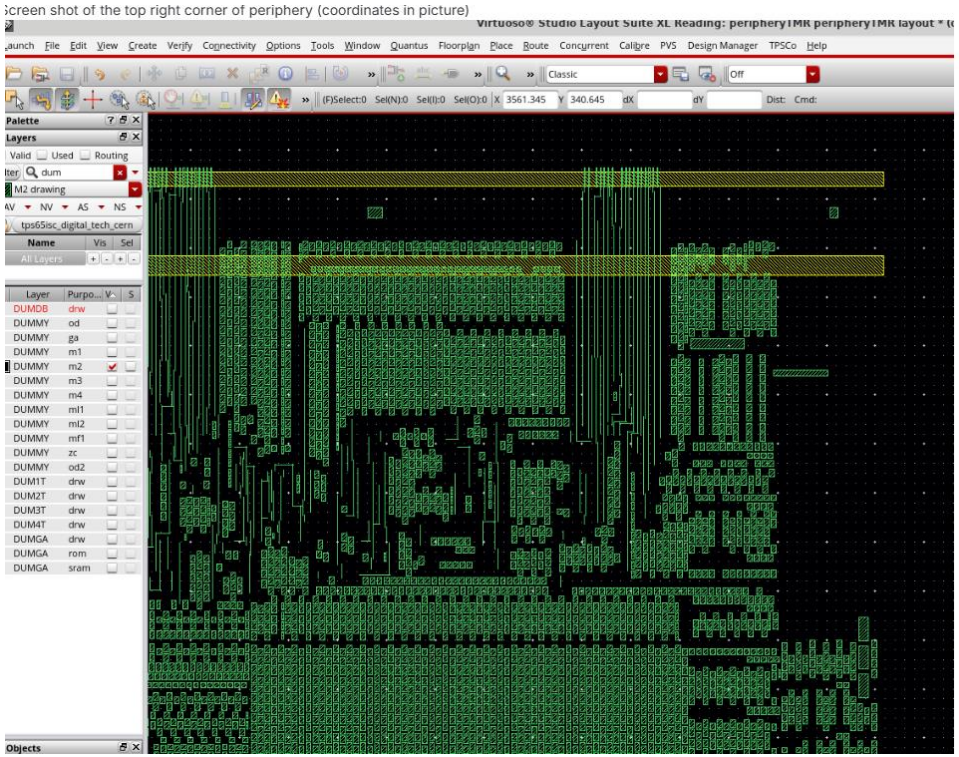
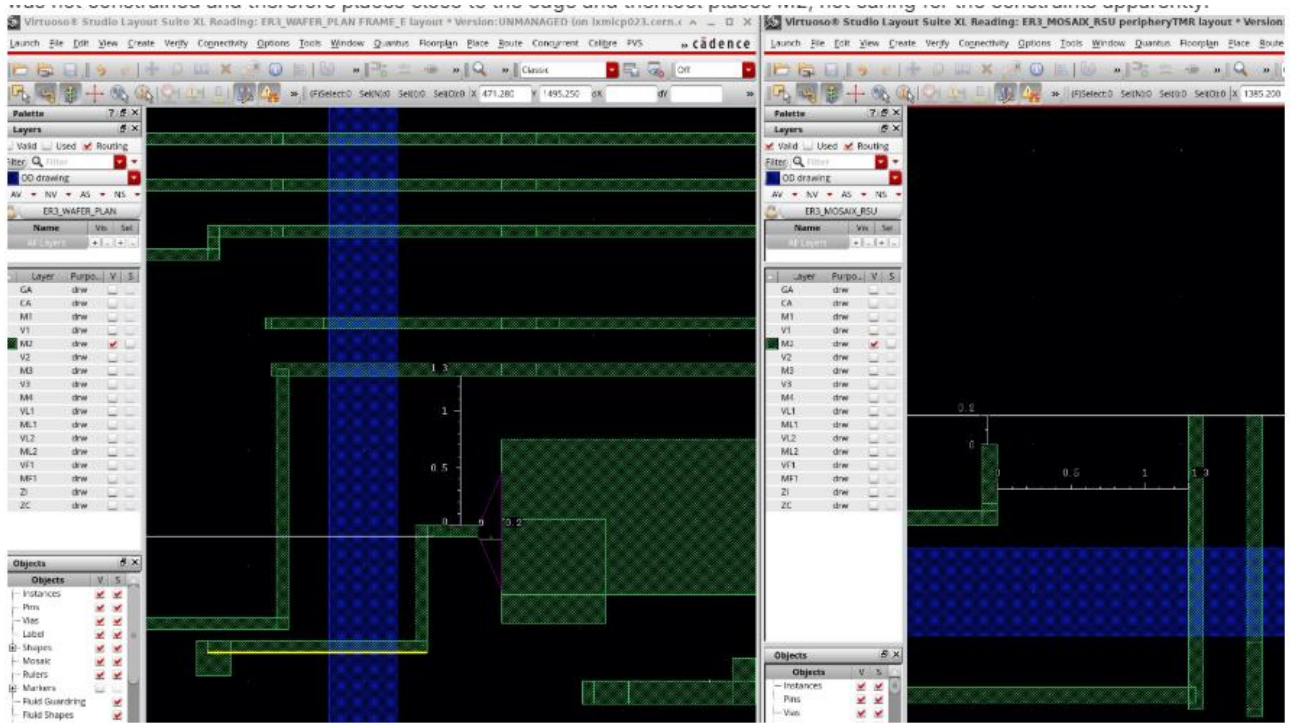
ER3 - Physcial layout work ongoing

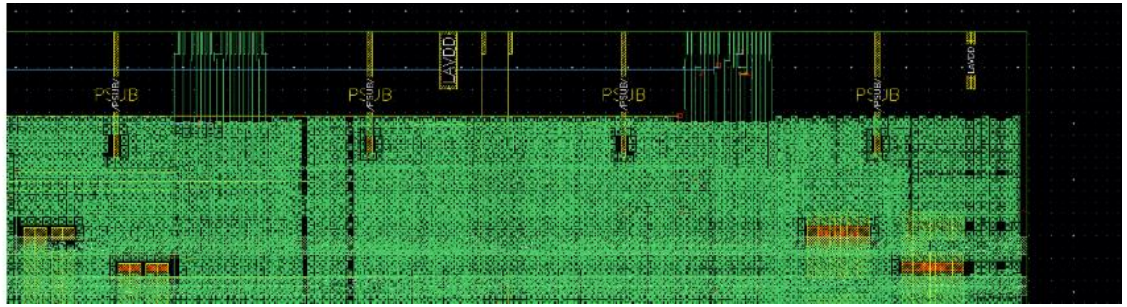


Problem with DRC filling density on the top right corner

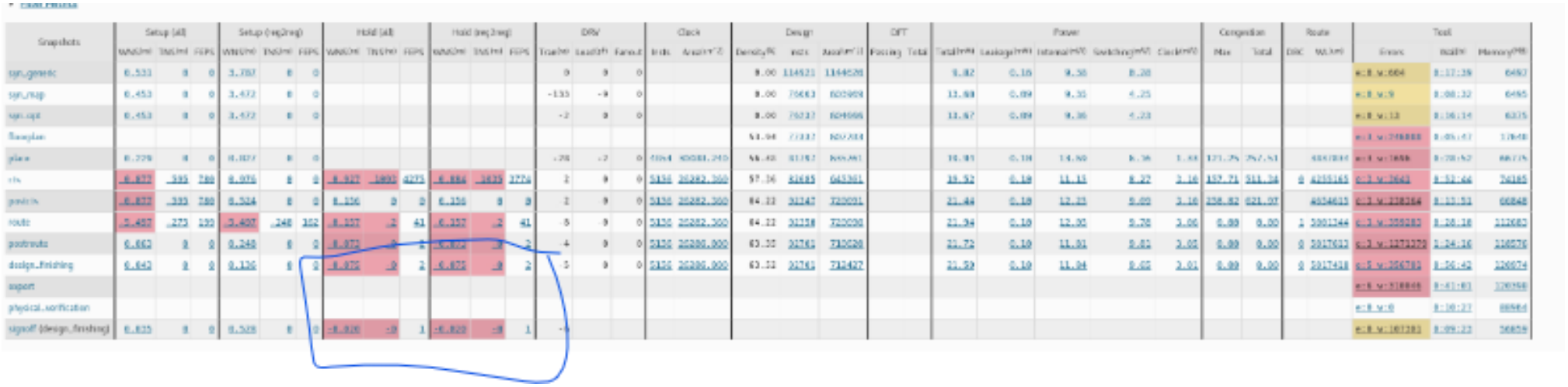


Problem on the RSU level : DRC violation on the interface between periphery and the matrix

First set of iterations



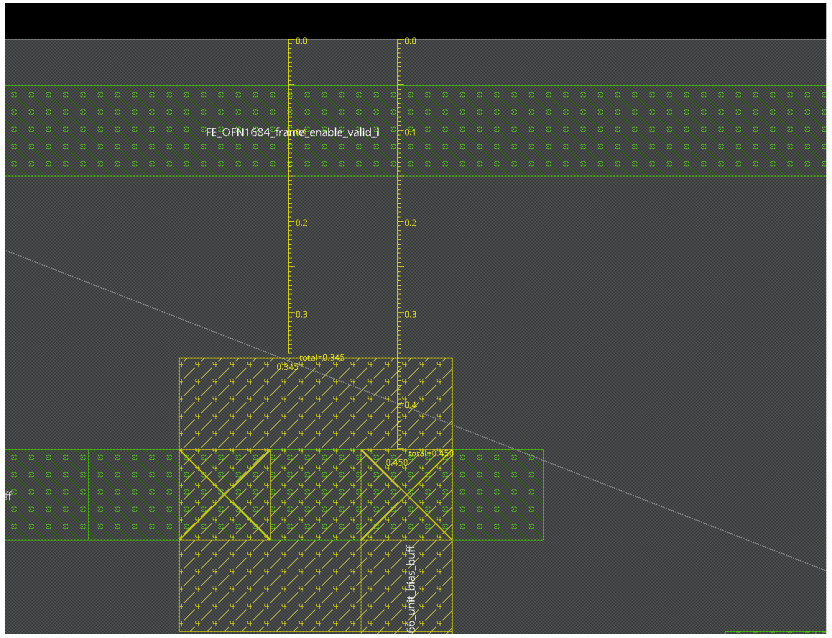
- Solving routing and the filling caused issues on the timing arcs



Second set of iterations

Snapshots	Setup (all)			Setup (reg2reg)			Hold (all)			Hold (reg2reg)			DRV			Clock		Design			DFT		Power					Congestion		Route	
	WNS(ns)	TNS(ns)	FEPS	WNS(ns)	TNS(ns)	FEPS	WNS(ns)	TNS(ns)	FEPS	WNS(ns)	TNS(ns)	FEPS	Tran(ns)	Load(pF)	Fanout	Insts	Area(um^2)	Density(%)	Insts	Area(um^2)	Passing	Total	Total(mW)	Leakage(mW)	Internal(mW)	Switching(mW)	Clock(mW)	Max	Total	DRC	WL(um)
syn_generic	0.531	0	0	3.787	0	0							0	0	0			0.00	114921	1144620			9.82	0.16	9.38	0.28					
syn_map	0.453	0	0	3.472	0	0							-133	-9	0			0.00	76063	603969			13.68	0.09	9.35	4.25					
syn_opt	0.453	0	0	3.472	0	0							-2	0	0			0.00	76237	604666			13.67	0.09	9.36	4.23					
floorplan																		53.94	77337	607783											
place	-0.032	-0	2	-0.032	-0	2							-24	-2	0	4863	30207.840	56.49	81786	635850			19.91	0.10	13.68	6.14	1.34	146.36	247.87		3817998
cts	-0.772	-514	780	1.223	0	0	-1.004	-1076	4337	-1.004	-1009	3455	-19	-2	0	5117	26024.960	57.28	82599	644404			19.50	0.10	11.14	8.26	3.07	203.61	436.59	0	4244197
postcts	-0.772	-514	780	0.581	0	0	0.162	0	0	0.190	0	0	-19	-2	0	5117	26024.960	64.04	92062	718080			21.31	0.10	12.23	8.98	3.07	282.95	625.64		4569593
route	-6.313	-520	320	-6.313	-486	280	-0.328	-38	322	-0.328	-38	322	-34	-2	0	5117	26024.960	64.04	92066	718086			21.76	0.10	12.04	9.61	3.02	0.00	0.00	36	4934689
postroute	0.042	0	0	0.187	0	0	0.052	0	0	0.052	0	0	-4	0	0	5117	26035.880	63.19	92355	708823			21.54	0.10	11.80	9.64	3.01	0.00	0.00	36	4948980
design_finishing	0.051	0	0	0.197	0	0	0.032	0	0	0.032	0	0	-5	0	0	5117	26035.880	63.19	92355	708823			21.35	0.10	11.78	9.47	2.96	0.00	0.00	59	4948964
export																															
physical_verification																															
signoff (design_finishing)	0.238	0	0	0.269	0	0	0.074	0	0	0.074	0	0	-6																		

Cleaned timing issues, but…



ER3 candidate release

- Currently:
  - Clean timing
  - Clean DRC filling
  - Clean DRCs between matrix and the periphery

  ➔Candidate release, now
  running gate level simulations with this revision
  doing power checks and IR analysis

- Adding several steps for more detailed reporting during the flow
  - CTS nets
  - Glitch analysis
  - Cleanup of the errors