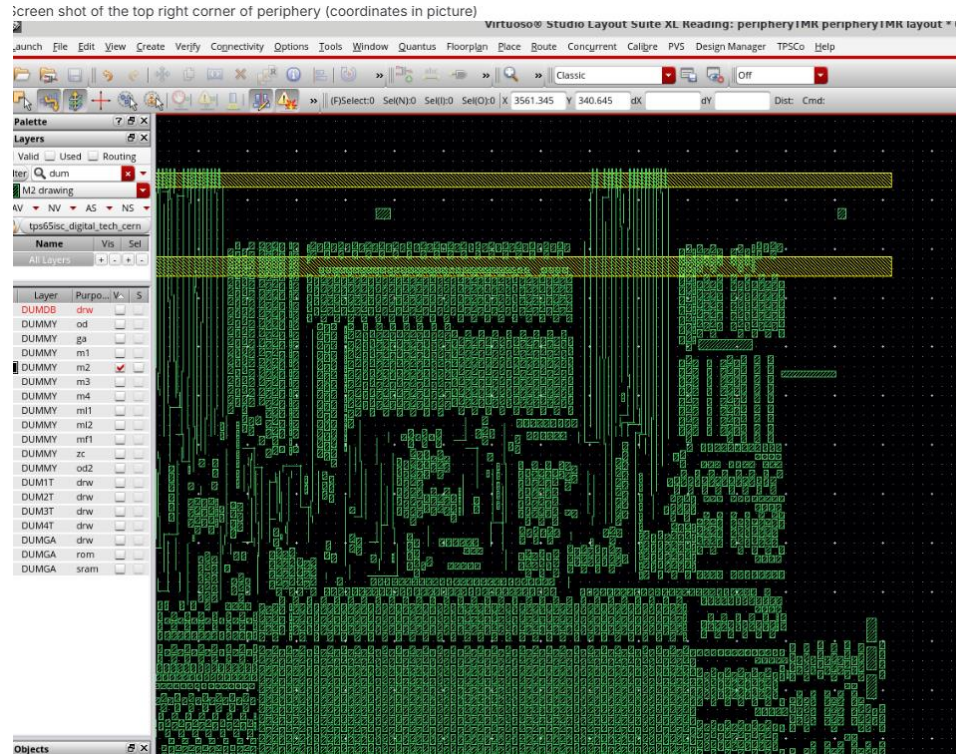


Update

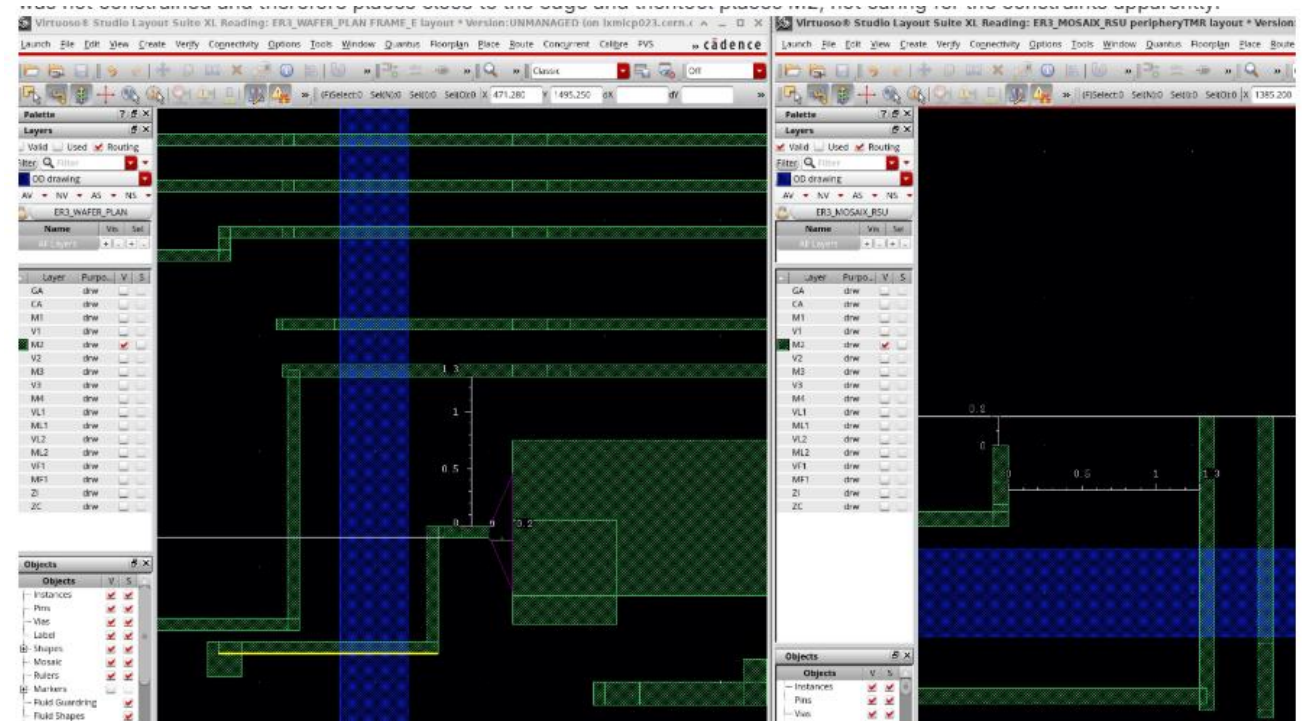
Jelena Lalic



ER3 - Physical layout work ongoing



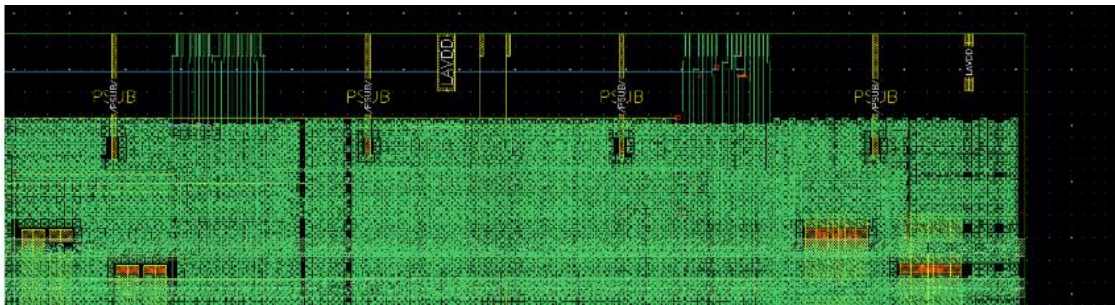
Problem with DRC filling density on the top right corner



Problem on the RSU level :
DRC violation on the interface between periphery and the matrix



First set of iterations



- Solving routing and the filling caused issues on the timing arcs

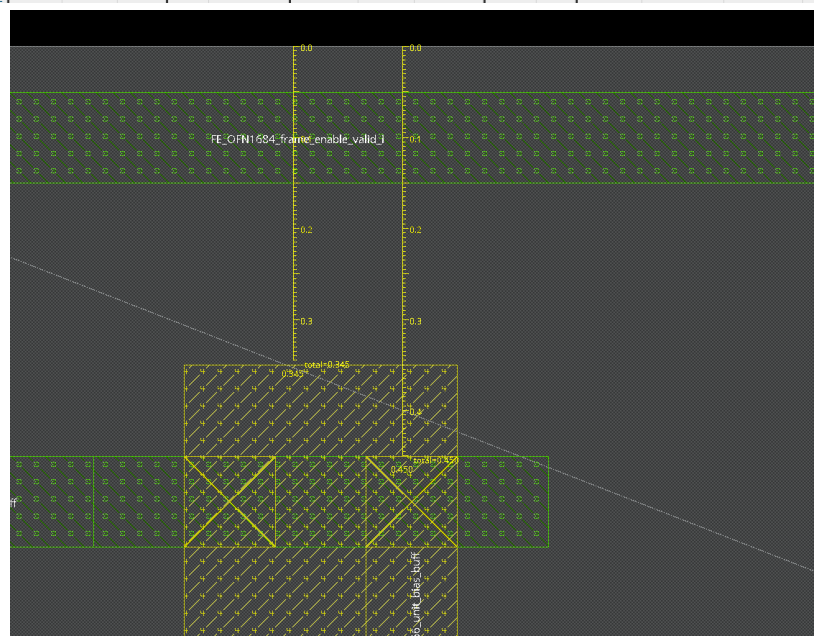
Snapshots	Setup (sB)			Setup (sq2wg)			Hold (sB)			Hold (sq2wg)			DRV			Clock		Design			DFT		Power					Congestion		Route			Test							
	WNSUM	TSUM	FGPS	WNSUM	TSUM	FGPS	WNSUM	TSUM	FGPS	WNSUM	TSUM	FGPS	Transter	Loadsh	Fanout	Tride	Asym%	Density%	intr	Asym%	Passing	Total	Total%	usage%	instanc%	switching%	clock%	Min	Total	DRC	WLM	Errors	Nodes	Memory%						
syn_genlec	6.533	0	0	3.787	0	0							0	0	0			8.00	114923	1144528																				
syn_top	6.453	0	0	3.472	0	0							-135	-8	0			8.00	76683	802958																				
syn_opt	6.453	0	0	3.472	0	0							-2	0	0			8.00	76723	804998																				
3waylas																		51.94	77337	1607034																				
place	6.778	0	0	0.027	0	0							-28	-2	0	1064	40081.245	48.48	81187	166381																				
rtx	-6.877	-335	280	0.976	0	0	-6.877	-1807	4275	-6.884	-1825	2724	2	0	0	5136	20282.360	57.36	81885	643361																				
pinvts	-6.877	-335	280	0.524	0	0	6.136	0	0	6.135	0	0	2	0	0	5136	20282.360	84.11	31147	720001																				
route	-5.487	-273	230	-3.407	-248	162	-6.137	-2	41	-6.137	-2	41	0	0	0	5136	20282.360	84.11	31138	720000																				
postroute	6.662	0	0	0.248	0	0	6.877	0	0	6.877	0	0	2	4	0	5136	20280.800	63.22	31745	732028																				
design_finishing	6.642	0	0	0.136	0	0	-6.875	-0	2	-6.875	-0	2	0	0	0	5136	20280.800	63.22	31745	732427																				
import																																								
physical_verification																																								
signoff (design_finishing)	6.825	0	0	0.528	0	0	-6.826	-0	1	-6.826	-0	1	-1	-1																										



Second set of iterations

Snapshots	Setup (all)			Setup (reg2reg)			Hold (all)			Hold (reg2reg)			DRV			Clock		Design			DFT		Power					Congestion		Route	
	WNS(ns)	TNS(ns)	FEPS	WNS(ns)	TNS(ns)	FEPS	WNS(ns)	TNS(ns)	FEPS	WNS(ns)	TNS(ns)	FEPS	Tran(ns)	Load(μF)	Fanout	Insts	Area(μm ²)	Density(%)	Insts	Area(μm ²)	Passing	Total	Total(mW)	Leakage(mW)	Internal(mW)	Switching(mW)	Clock(mW)	Max	Total	DRC	WL(μm)
syn_generic	0.531	0	0	3.787	0	0							0	0	0			0.00	114921	1144620			9.82	0.16	9.38	0.28					
syn_map	0.453	0	0	3.472	0	0							-133	-9	0			0.00	76063	603969			13.68	0.09	9.35	4.25					
syn_opt	0.453	0	0	3.472	0	0							-2	0	0			0.00	76237	604666			13.67	0.09	9.36	4.23					
floorplan																		53.94	77337	607783											
place	-0.032	-0	2	-0.032	-0	2							-24	-2	0	4863	30207.840	56.49	81786	635850			19.91	0.10	13.68	6.14	1.34	146.36	247.87	3817998	
cts	-0.772	-514	780	1.223	0	0	-1.004	-1076	4337	-1.004	-1009	3455	-19	-2	0	5117	26024.960	57.28	82599	644404			19.50	0.10	11.14	8.26	3.07	203.61	436.59	0	4244197
postcts	-0.772	-514	780	0.581	0	0	0.162	0	0	0.190	0	0	-19	-2	0	5117	26024.960	64.04	92062	718080			21.31	0.10	12.23	8.98	3.07	282.95	625.64	4569593	
route	-6.313	-520	320	-6.313	-486	280	-0.328	-38	322	-0.328	-38	322	-34	-2	0	5117	26024.960	64.04	92066	718086			21.76	0.10	12.04	9.61	3.02	0.00	0.00	36	4934689
postroute	0.042	0	0	0.187	0	0	0.052	0	0	0.052	0	0	-4	0	0	5117	26035.880	63.19	92355	708823			21.54	0.10	11.80	9.64	3.01	0.00	0.00	36	4948980
design_finishing	0.051	0	0	0.197	0	0	0.032	0	0	0.032	0	0	-5	0	0	5117	26035.880	63.19	92355	708823			21.35	0.10	11.78	9.47	2.96	0.00	0.00	59	4948964
export																															
physical_verification																															
signoff (design_finishing)	0.238	0	0	0.269	0	0	0.074	0	0	0.074	0	0	-6																		

Cleaned timing issues, but...





ER3 candidate release

- Currently:
 - Clean timing
 - Clean DRC filling
 - Clean DRCs between matrix and the periphery
 - ➔ Candidate release, now running gate level simulations with this revision doing power checks and IR analysis
- Adding several steps for more detailed reporting during the flow
 - CTS nets
 - Glitch analysis
 - Cleanup of the errors