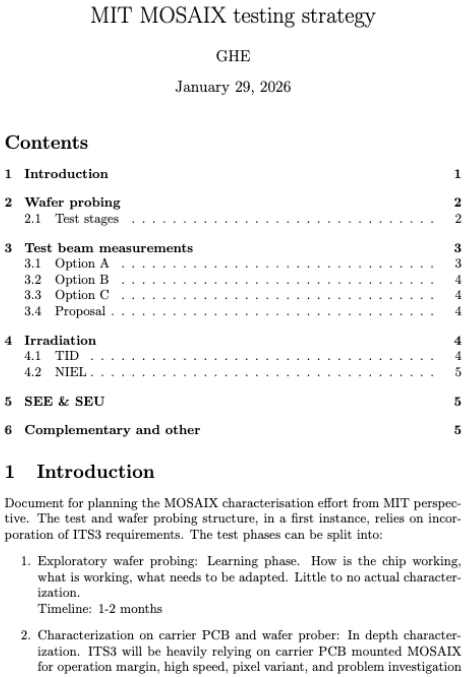
Status update

- Installed hardware at wafer prober with Stefano
  - Small adjustments and extensions expected (missing one SMU)
  - Communication between DAQ pc and instrumnets next
  - We need to make power adapter cables for our probecard (not super urgent, to note down)
- Some hardware change in cabling and sw adaption necessary for impedance measurement:
  - Will help with that.
- Dry run expected next week: ITS3 core devs had meeting this week -> found bugs (good) and we will have session together next week were we (MIT) try to dry run with them observing/helping (to see where there are more bugs
- Wafer prober add ons:
  - Looked at available sources in DSF -> standard cylindrical sources, easy to integrate
  - Requested quote for 500MBq Fe55 source (not yet received)
  - New idea: Investigate addition of X-Ray source for in-situ TID measurements on-wafer (could black box be compatible already, or made compatible)
    - Temperature controlled chuck options

Status update

- Started MIT MOSAIX testing strategy doc----->
  - Work in progress
- Cables arrived for future probe card investigation
  - VNA and PRBS measurement adapter cards to be made
- Open point of handling, loading, and contacting thinned chips (also within ITS3)
  - We need to have this skill, so I propose I start thinking (have some ideas)
- Papers:
  - Large MOSS paper accepted after revision: https://www.sciencedirect.com/science/article/pii/S0168900226000239
  - Metal stack paper came back with minor revisions (IEEE, me writing it): nearly there, however need feedback from Walter (deadline Monday)



MIT MOSAIX testing strategy

GHE

January 29, 2026

Contents

1 Introduction

Document for planning the MOSAIX characterisation effort from MIT perspective. The test and wafer probing structure, in a first instance, relies on incorporation of ITS3 requirements. The test phases can be split into:

1. Exploratory wafer probing: Learning phase. How is the chip working, what is working, what needs to be adapted. Little to no actual characterization.
   Timeline: 1-2 months
2. Characterization on carrier PCB and wafer prober: In depth characterization. ITS3 will be heavily relying on carrier PCB mounted MOSAIX for operation margin, high speed, pixel variant, and problem investigation