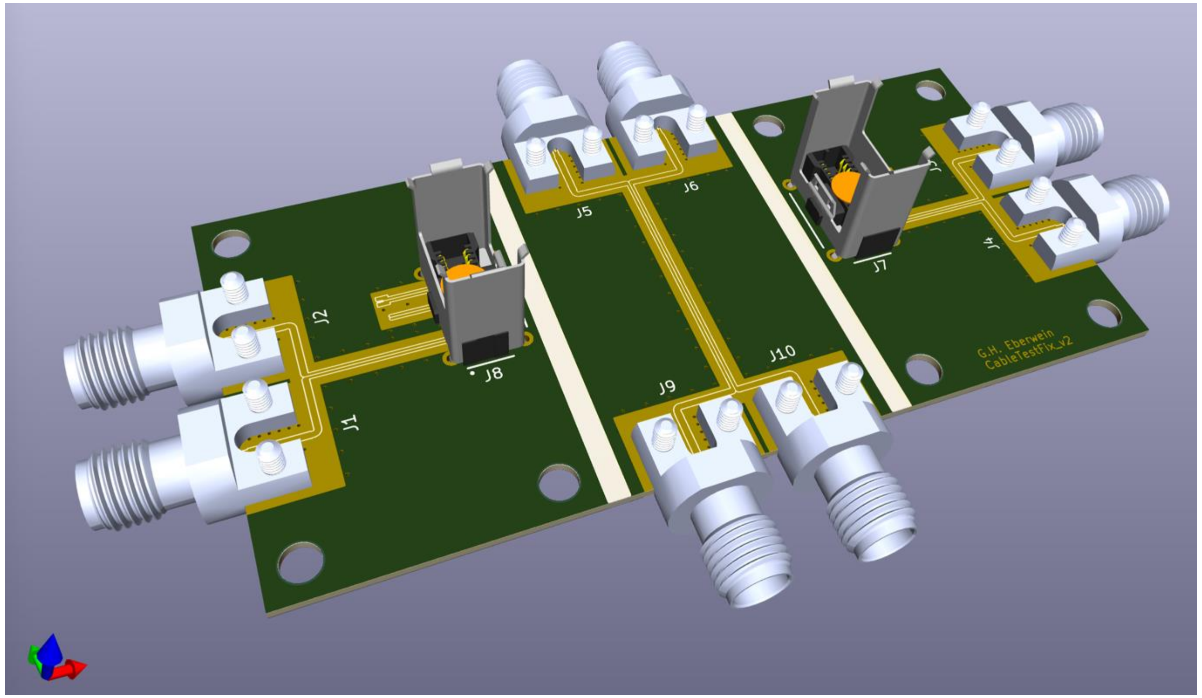
# Status update

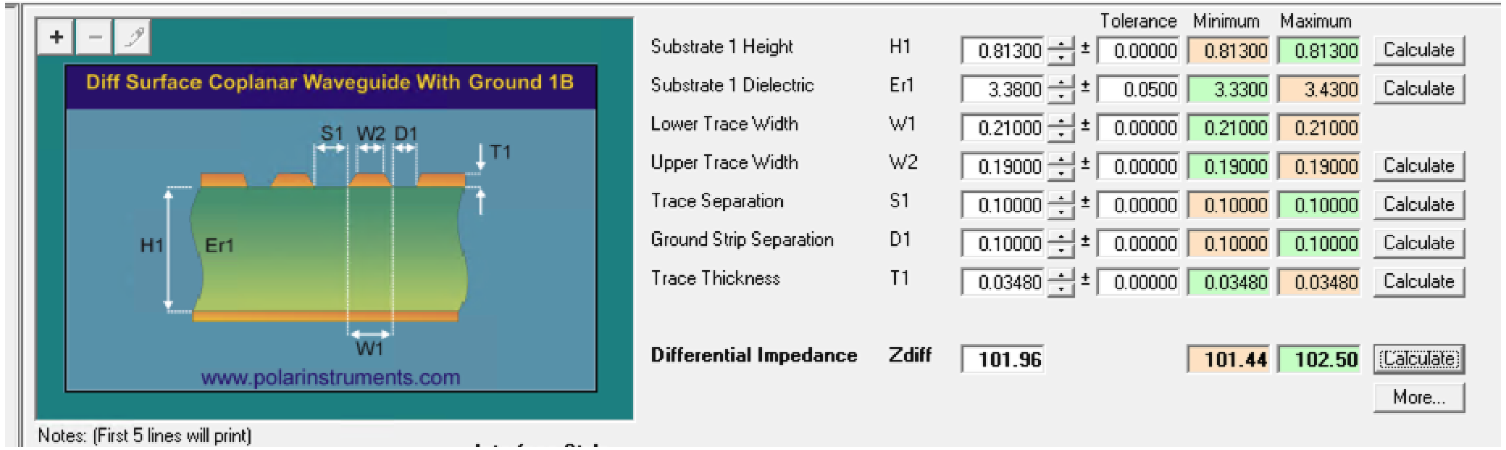
- Training session yesterday with ITS3 on software:
  - Re-run ourselves at wafer prober (setting up configurations now)
  - Support ITS3 for readiness -> chips arrive as soon as next week (I am not here Wed-Fr next week)
    - Impedance and powering
    - Feedback on dry-running the sowftware
    - Then focus on tasks on high-speed (writing tests and debugging tests) -> very useful as this is how we actually learn how to operate the chip compared to being just users of the test software
- Open point of handling, loading, and contacting thinned chips (also within ITS3)
  - We need to have this skill, so I propose I start thinking (have some ideas)
    - Not priority right now

- Papers:
  - Metal stack paper came back with minor revisions (IEEE, me writing it): nearly there, however need feedback from Walter (finally got feedback today, finalize this week)
- Conferences - discuss

# Status update

- Cables arrived for future probe card investigation
  - V2 of test fixture designed with feedback from Antoine and simulations from Stefano
  - Ordering today
  - Lower priority now – good to have available to learn tools





| | | | Tolerance | Minimum | Maximum | |
|---|---|---|---|---|---|---|
| Substrate 1 Height | H1 | 0.81300 | ± 0.00000 | 0.81300 | 0.81300 | Calculate |
| Substrate 1 Dielectric | Er1 | 3.3800 | ± 0.0500 | 3.3300 | 3.4300 | Calculate |
| Lower Trace Width | W1 | 0.21000 | ± 0.00000 | 0.21000 | 0.21000 | |
| Upper Trace Width | W2 | 0.19000 | ± 0.00000 | 0.19000 | 0.19000 | Calculate |
| Trace Separation | S1 | 0.10000 | ± 0.00000 | 0.10000 | 0.10000 | Calculate |
| Ground Strip Separation | D1 | 0.10000 | ± 0.00000 | 0.10000 | 0.10000 | Calculate |
| Trace Thickness | T1 | 0.03480 | ± 0.00000 | 0.03480 | 0.03480 | Calculate |
| **Differential Impedance** | **Zdiff** | 101.96 | | 101.44 | 102.50 | Calculate |
| | | | | | | More... |

Notes: (First 5 lines will print)