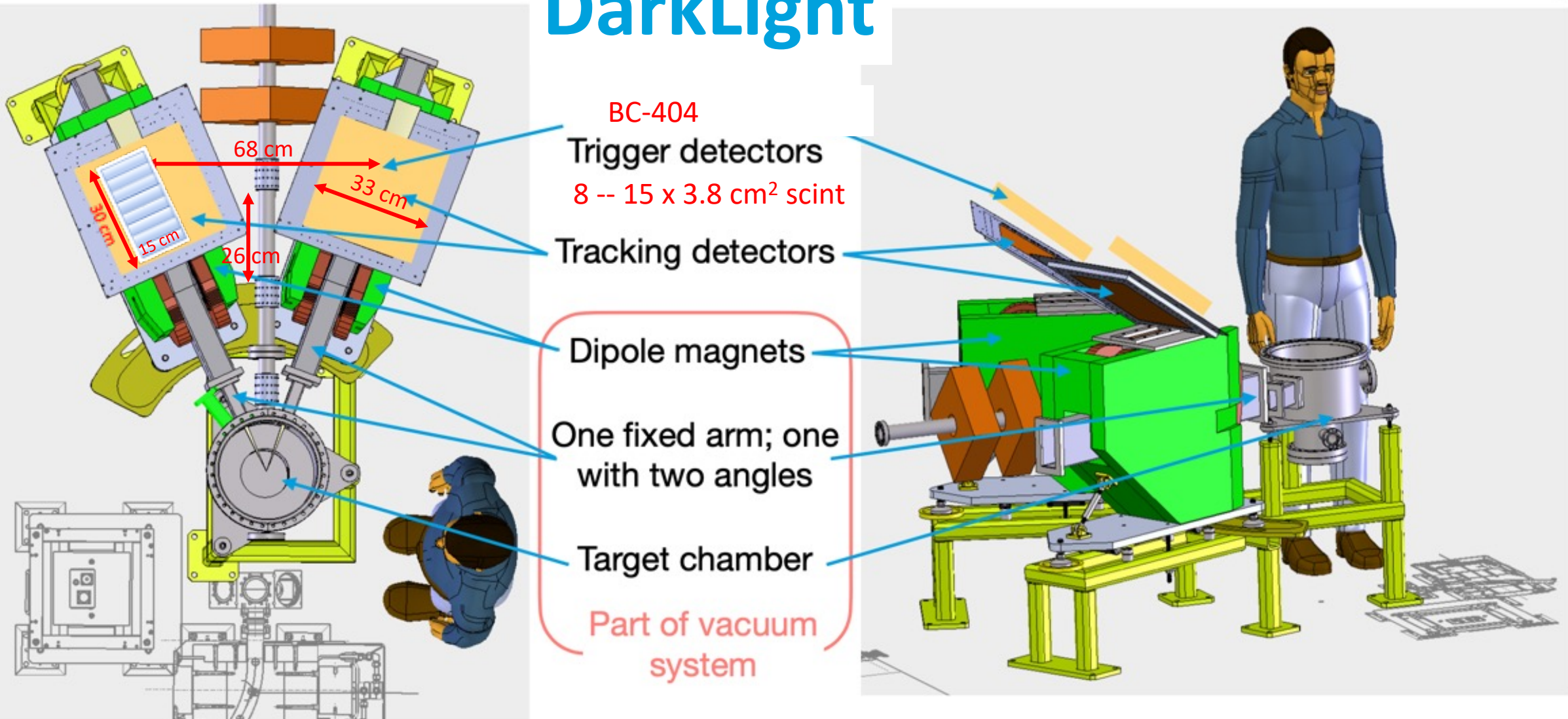
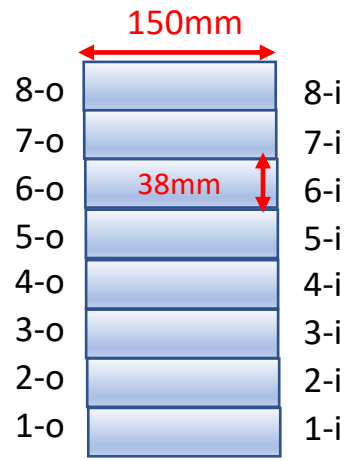


The experimental apparatus

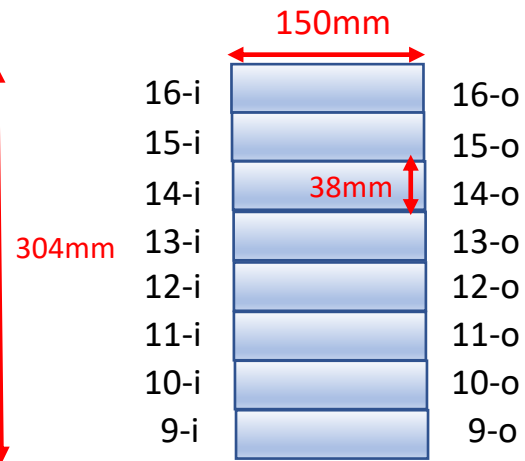
DarkLight



electron (3.6 MHz)



positron (30 kHz)



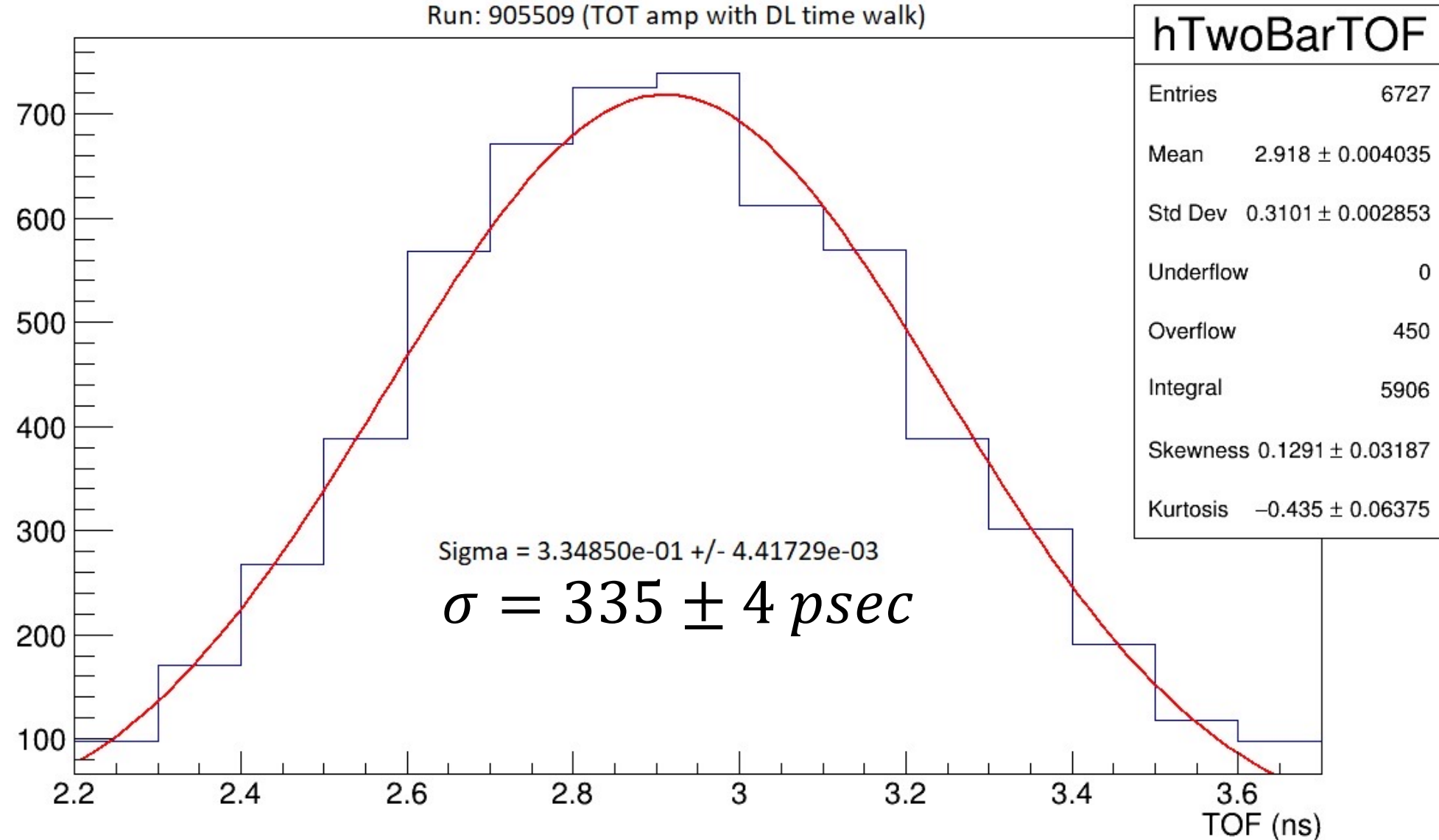
Different FPGA programs required

1. Need to be able to trigger on single counters for calibration.
2. Need to adjust timing for each counter to account for the different path lengths in the spectrometers.
3. Need to form **L-R coincident** triggers for each bar, then form **OR** of 8 e- bars, 8 e+ bars, then trigger e- * e+
4. Need to generate the fast trigger for readout of the GEM tracking chambers – within 1 usec (??)
4. For each of the 16 scintillators that have signals above threshold –
 - make in-out coincidence
 - make electron – positron coincidence (want < 200 psec time resolution)
 - output LE and TE time for an offline time walk correction

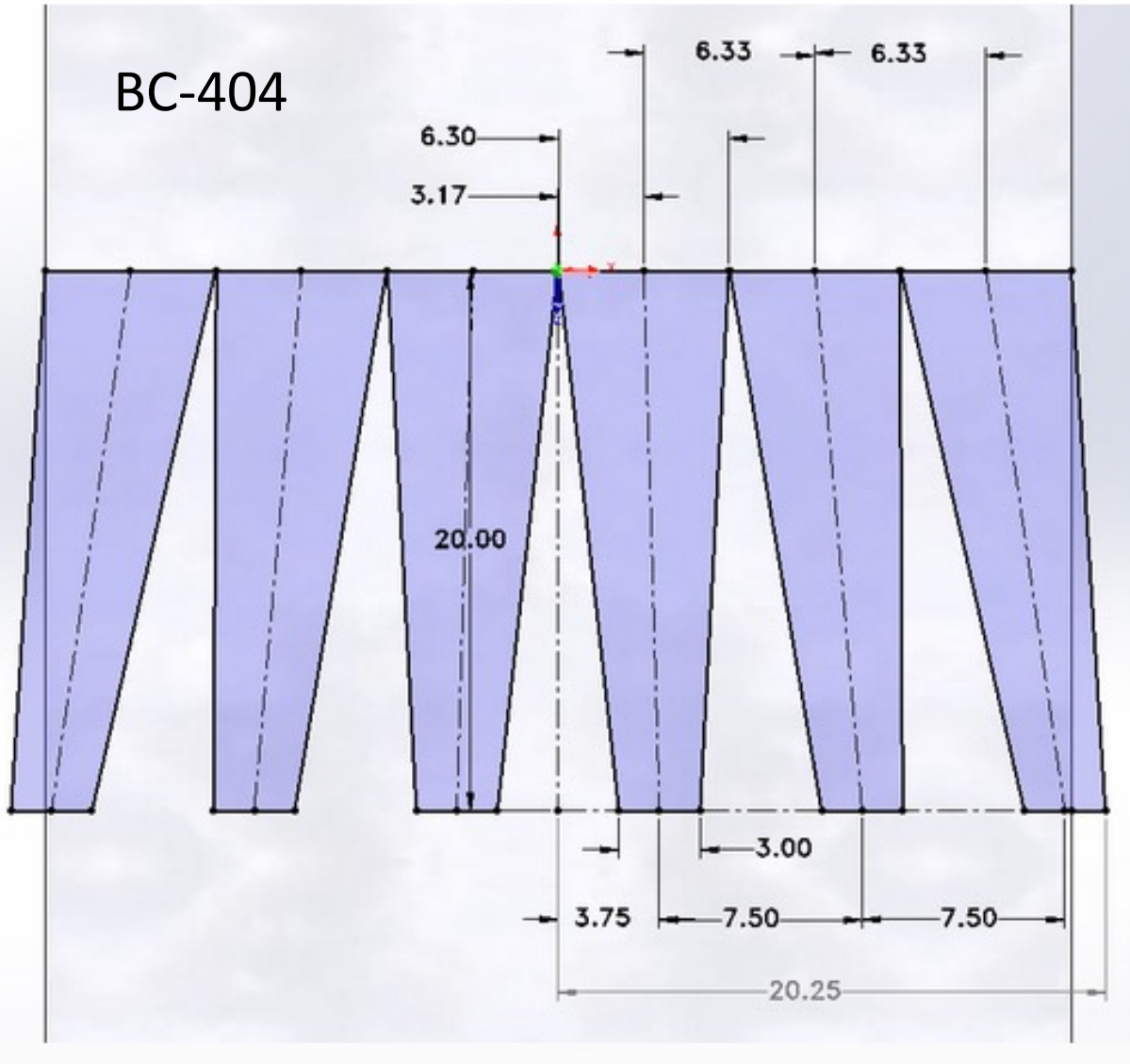
TOF Alpha bar with #1 DL Prototype Bar

Time of flight between two bars

Run: 905509 (TOT amp with DL time walk)



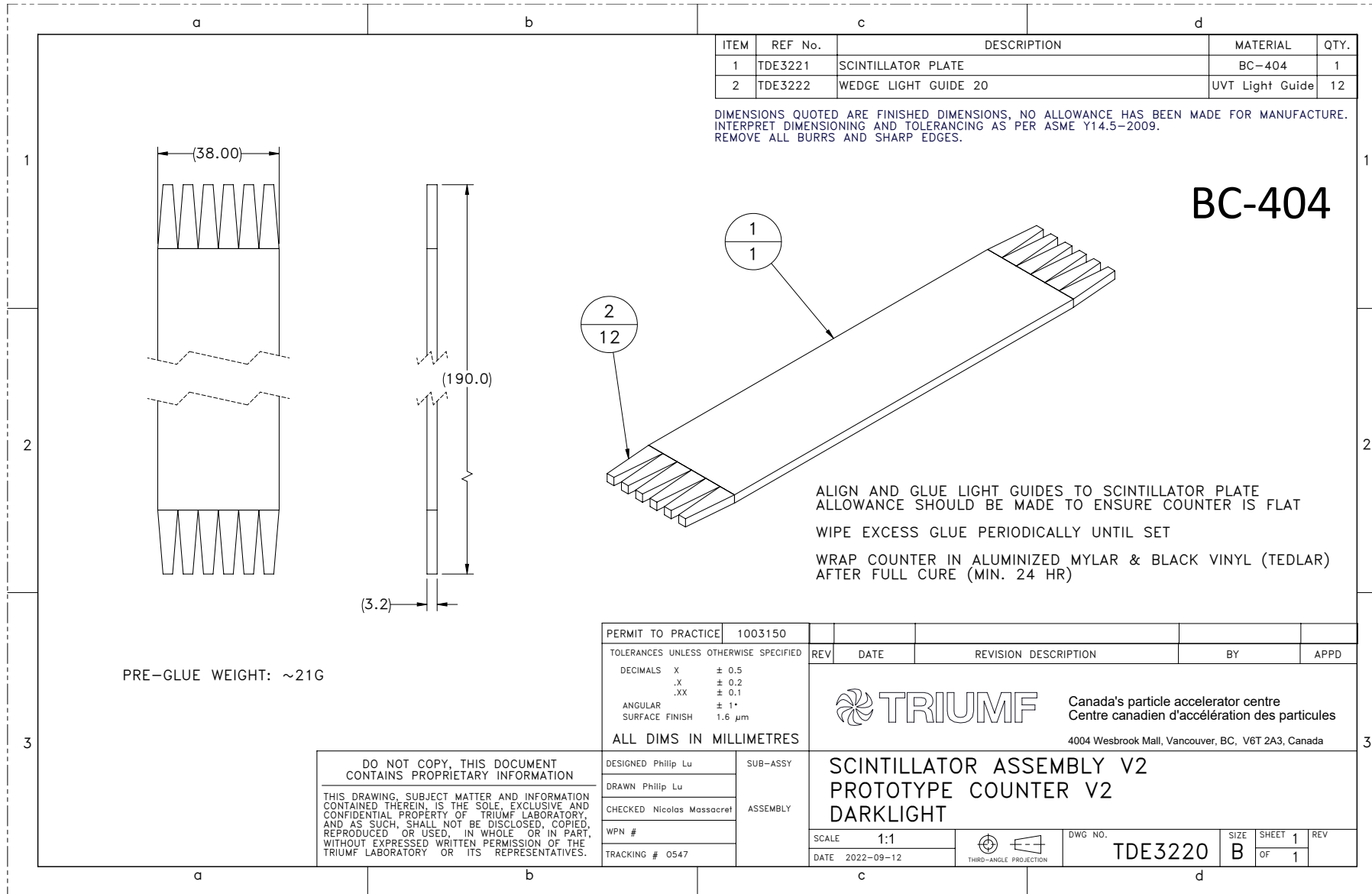
v1b -- 6 SiPM DarkLight Scintillator 38mm wide



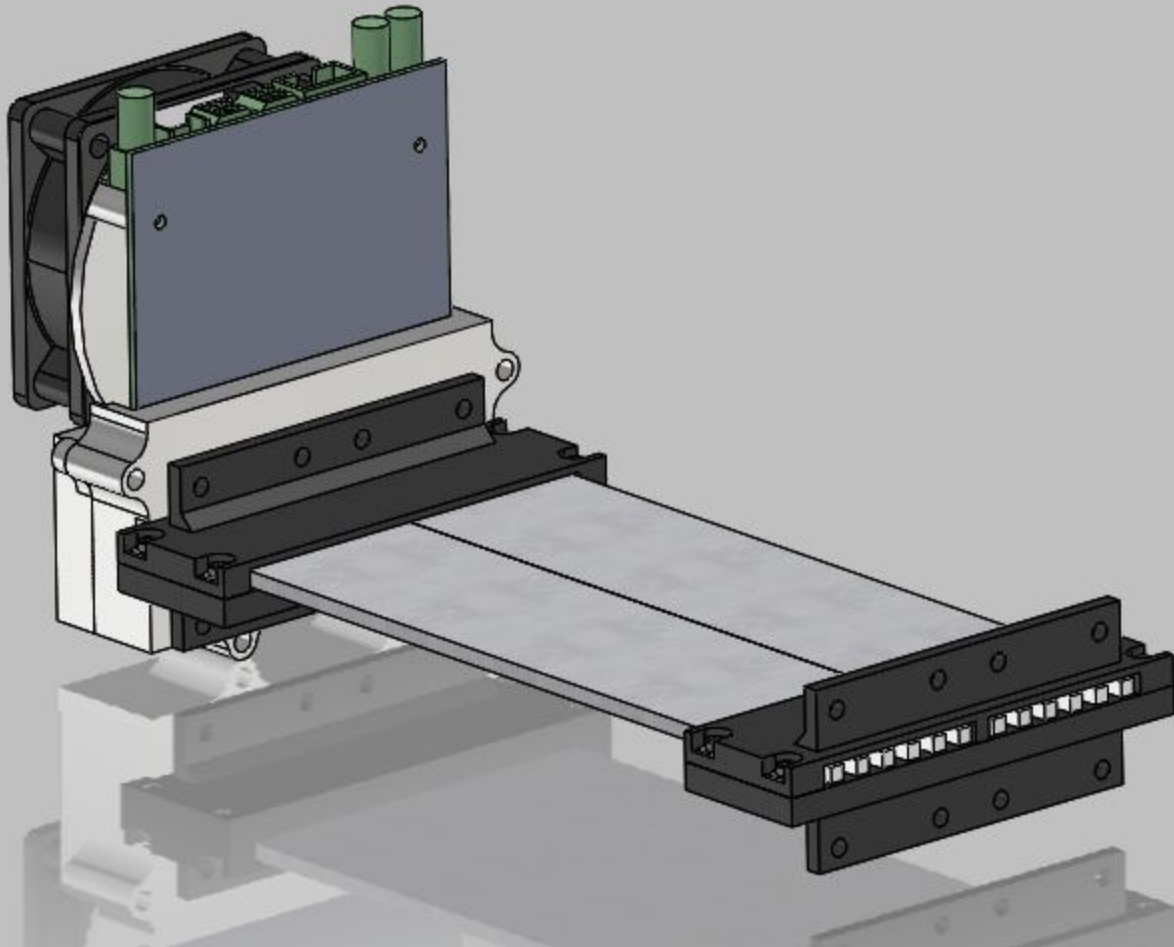
SiPM spacing at 7.50mm to match the existing frontend readout board designed for 4 SiPMs on 30mm scintillator

-- not tested

v2 -- 6 SiPM DarkLight Scintillator 38mm wide



v2-- Prototype Scintillator May 2023

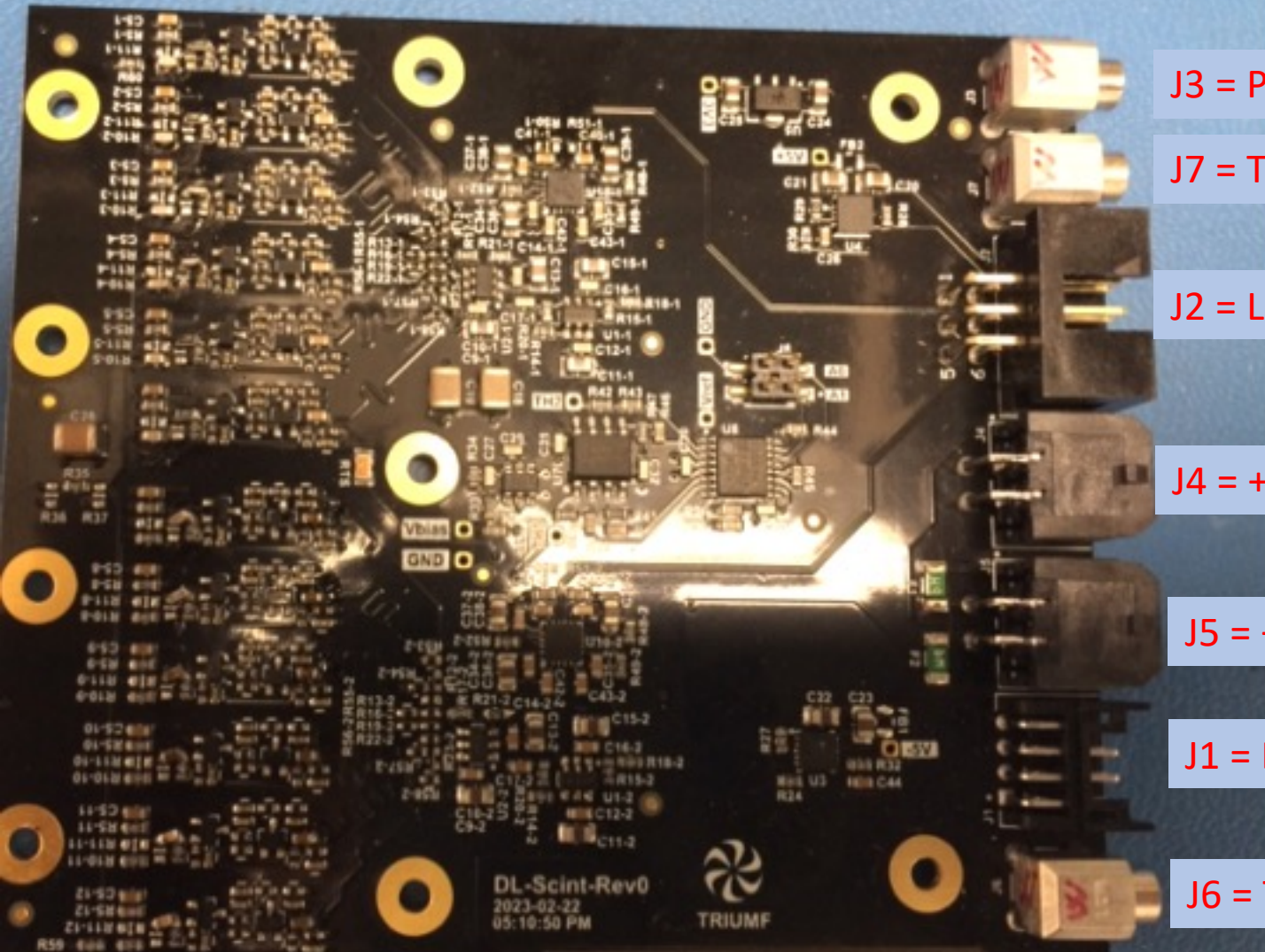


38 mm wide with 6 SiPMs at each end

One Electronic card holds
2 scintillators and 12 SiPMs

NEW v2 front end readout card (top side)

Preamp, Sum Amp, Discriminator



J3 = Pulser-in

J7 = TS1 out

J2 = Logic Out

J4 = +/-5V

J5 = +/-5V

J1 = BIAS 55 V

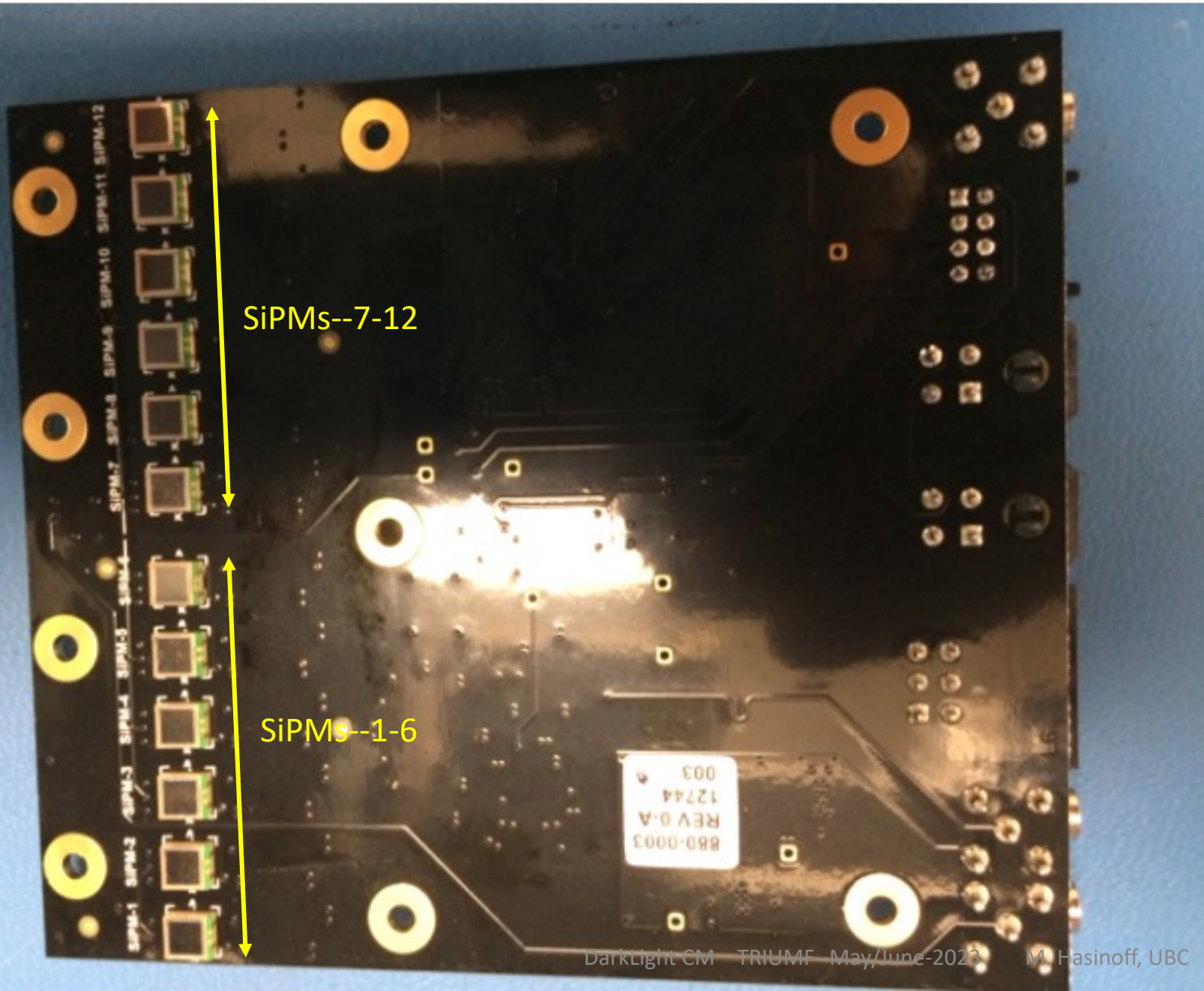
J6 = TS2 out

- holds 12 SiPMs/2 scintillators
- SUM(6) → fast amp → discriminator
- FPGA will check e+ e- coincidence
- FPGA will readout LE and TE time

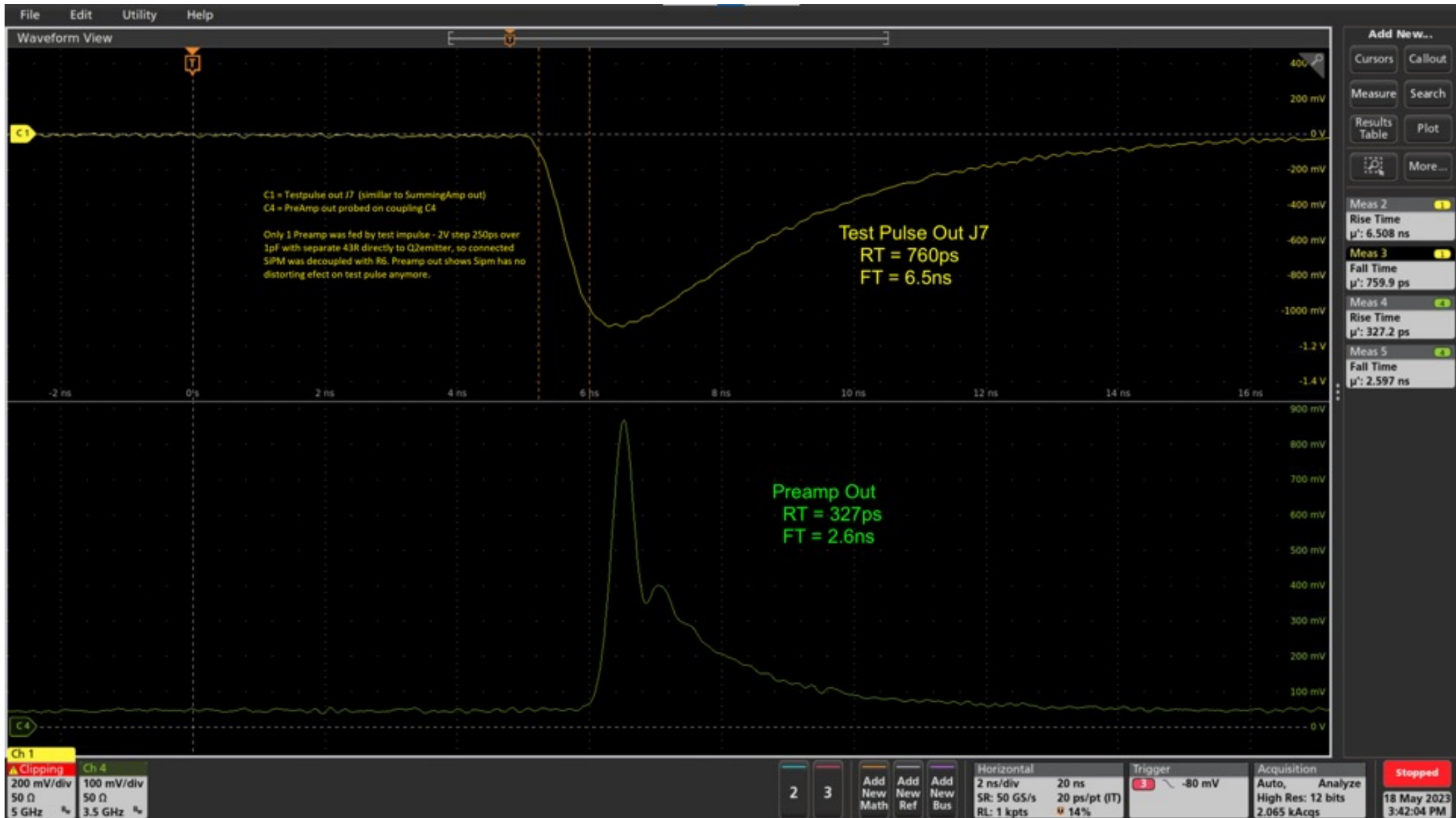
Next Stages—

- measure time resolution (L-R)
- measure time resolution -- 2 bars
- design power dist'n board
- design test pulse dist'n system
- develop trigger FPGA system

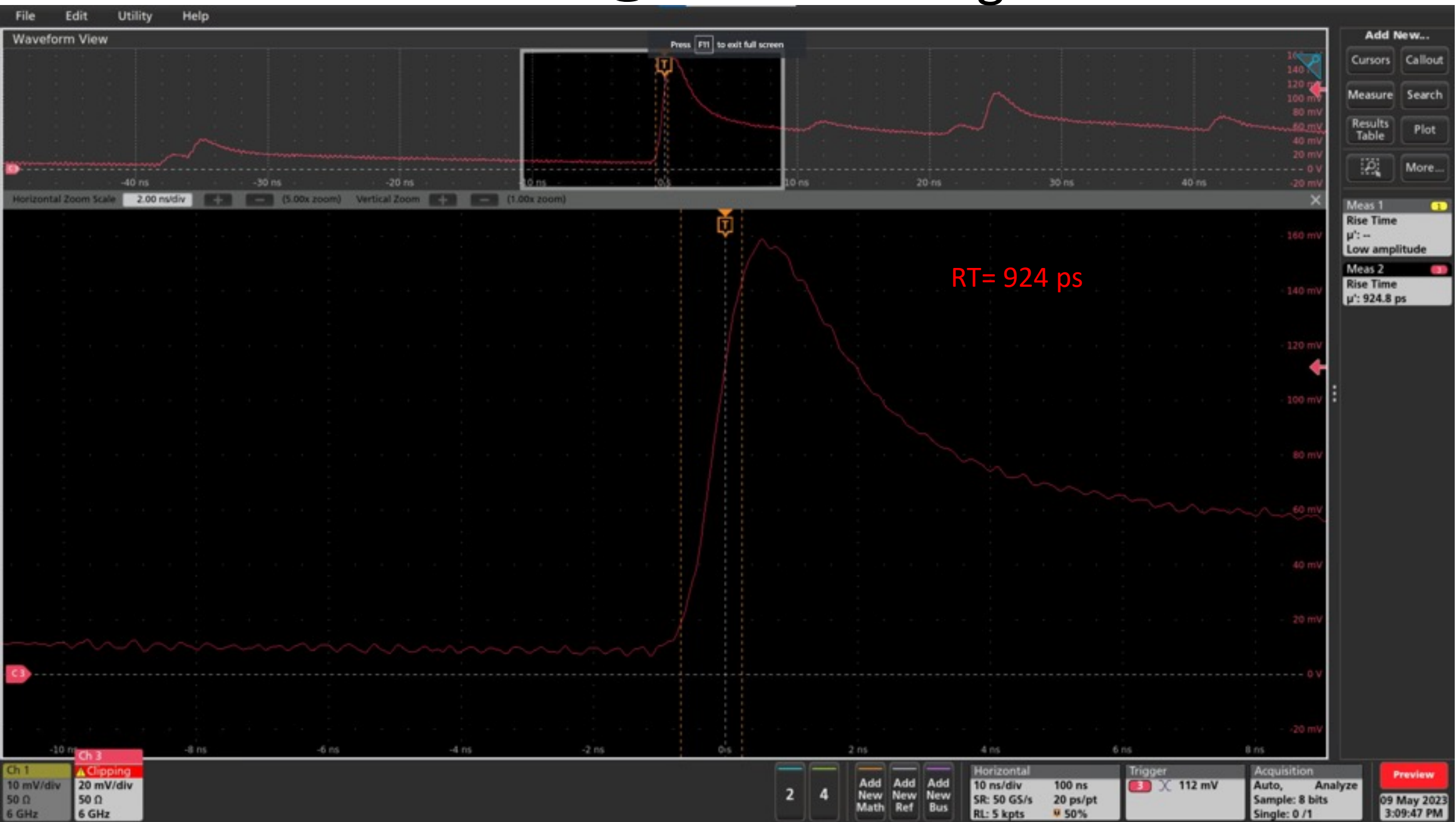
NEW v2 front end readout card (bottom side)

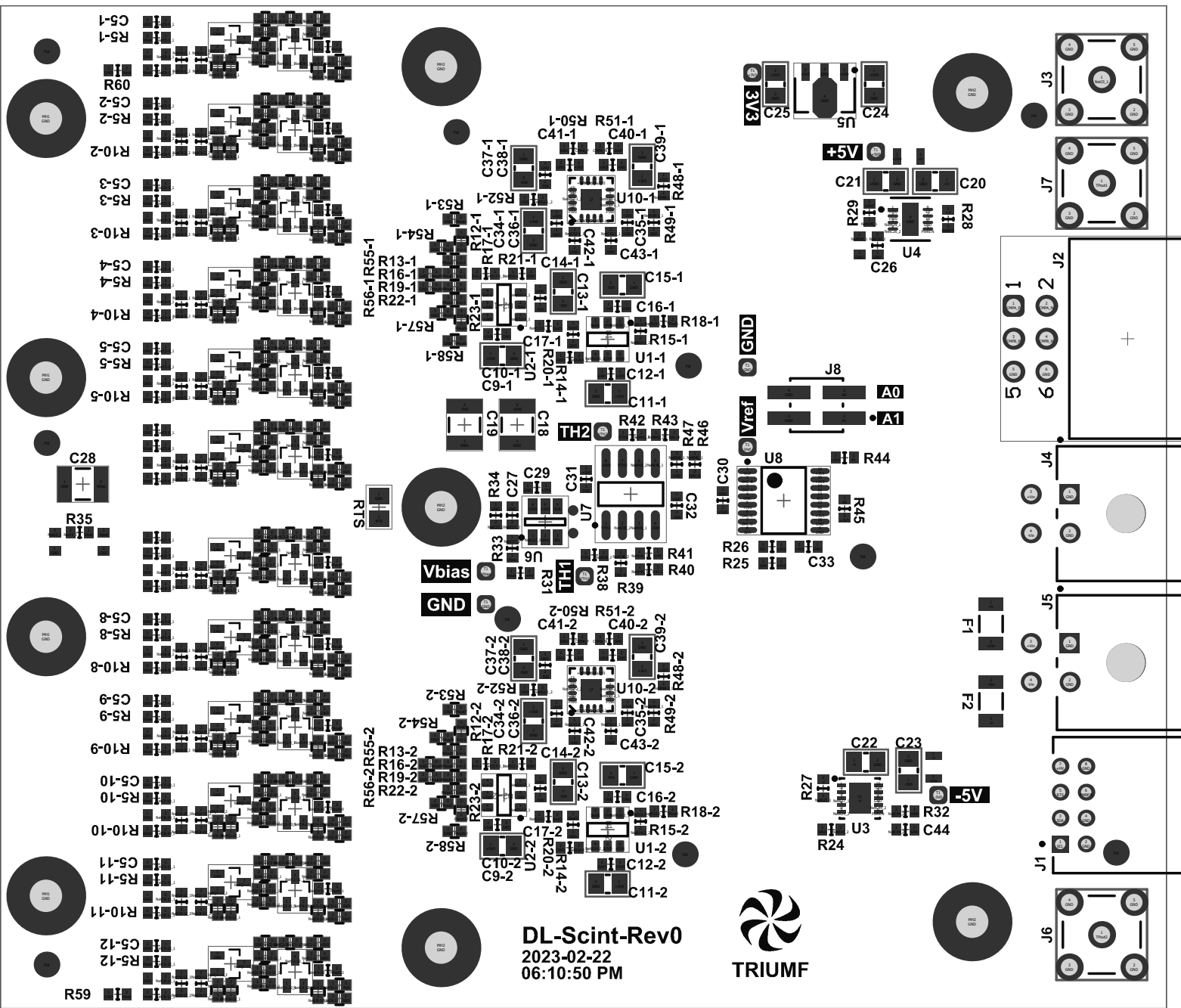


Square wave Test Input pulse



SiPM Dark Noise @ 8V overvoltage





MCX output connectors

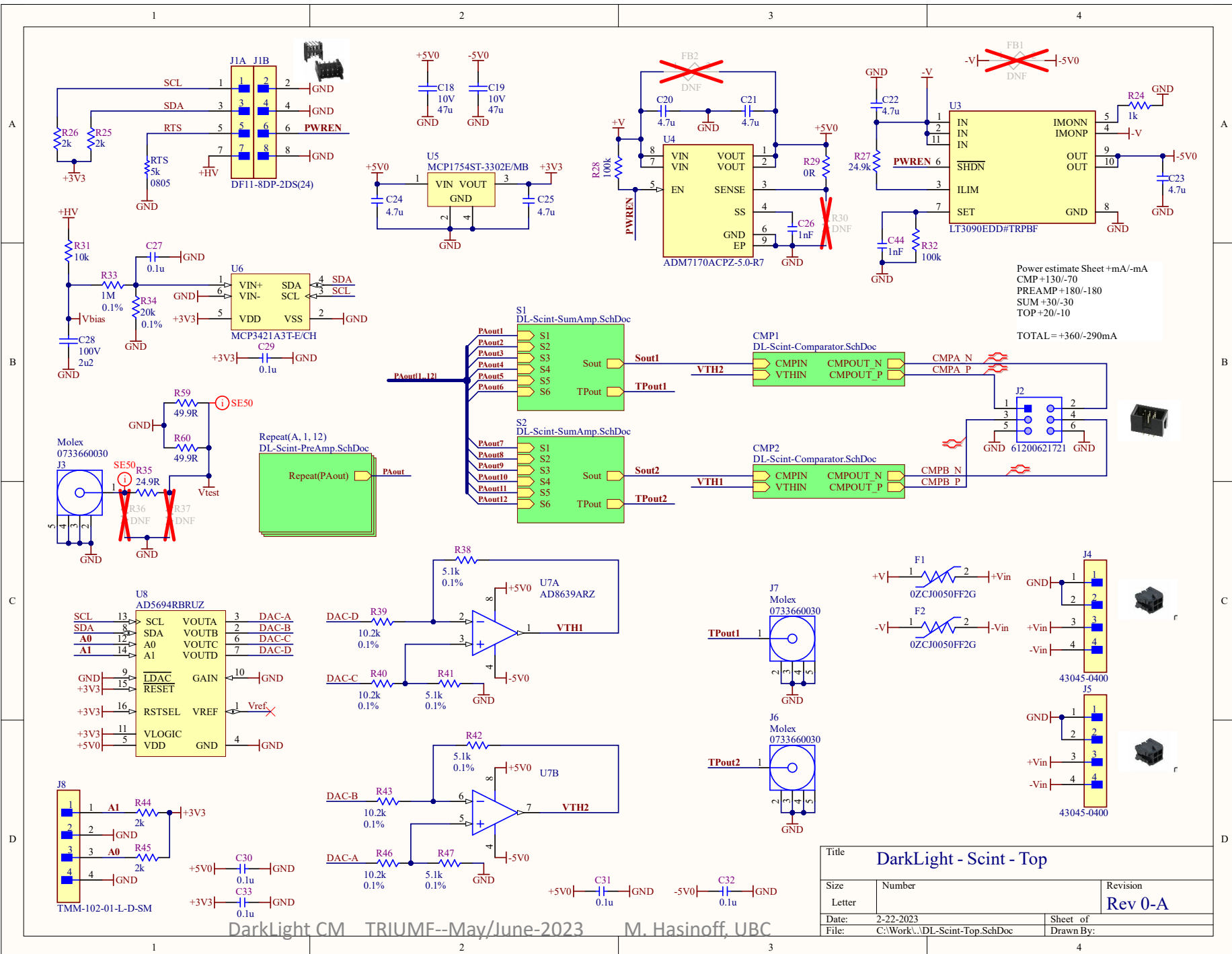
DL-Scint-Rev0
 2023-02-22
 06:10:50 PM



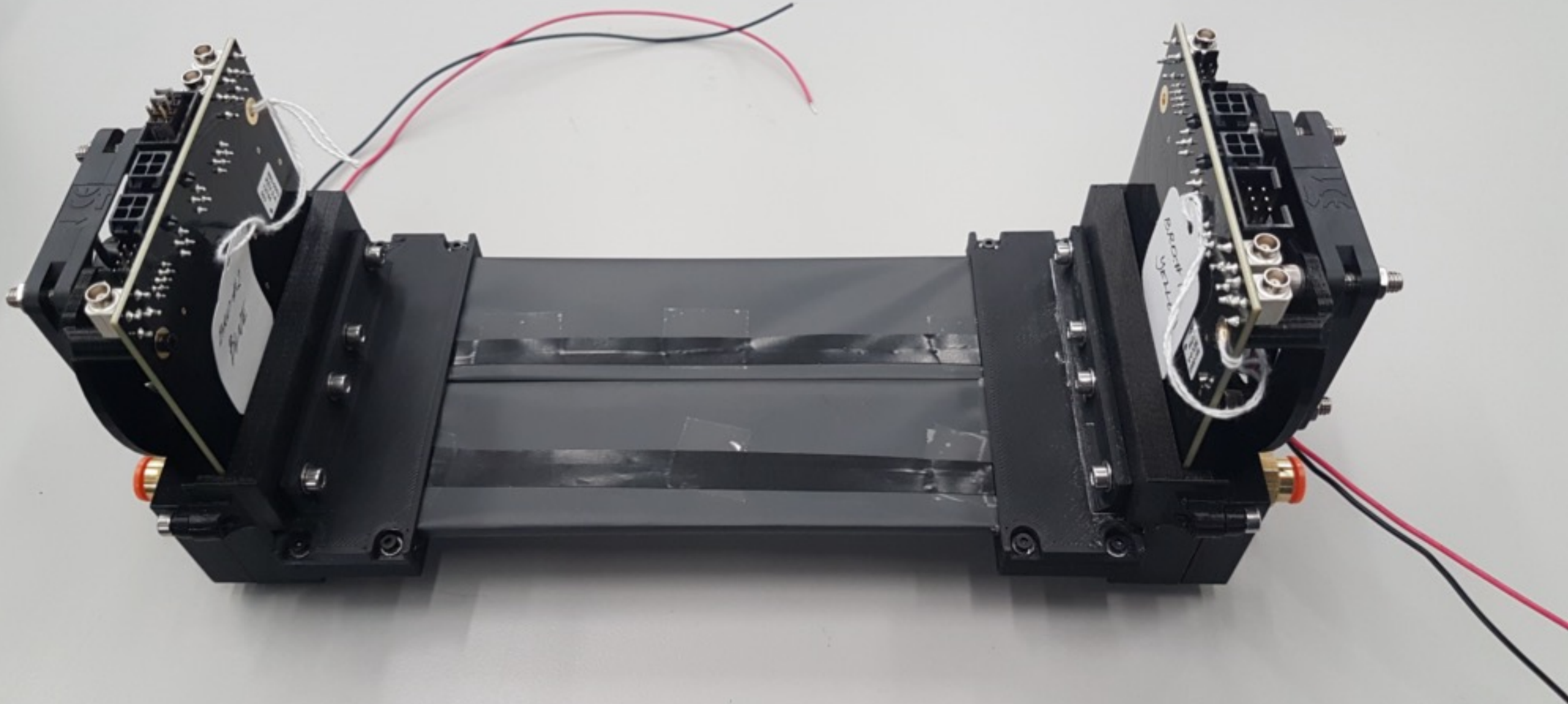
v2- Schematic

May 2023

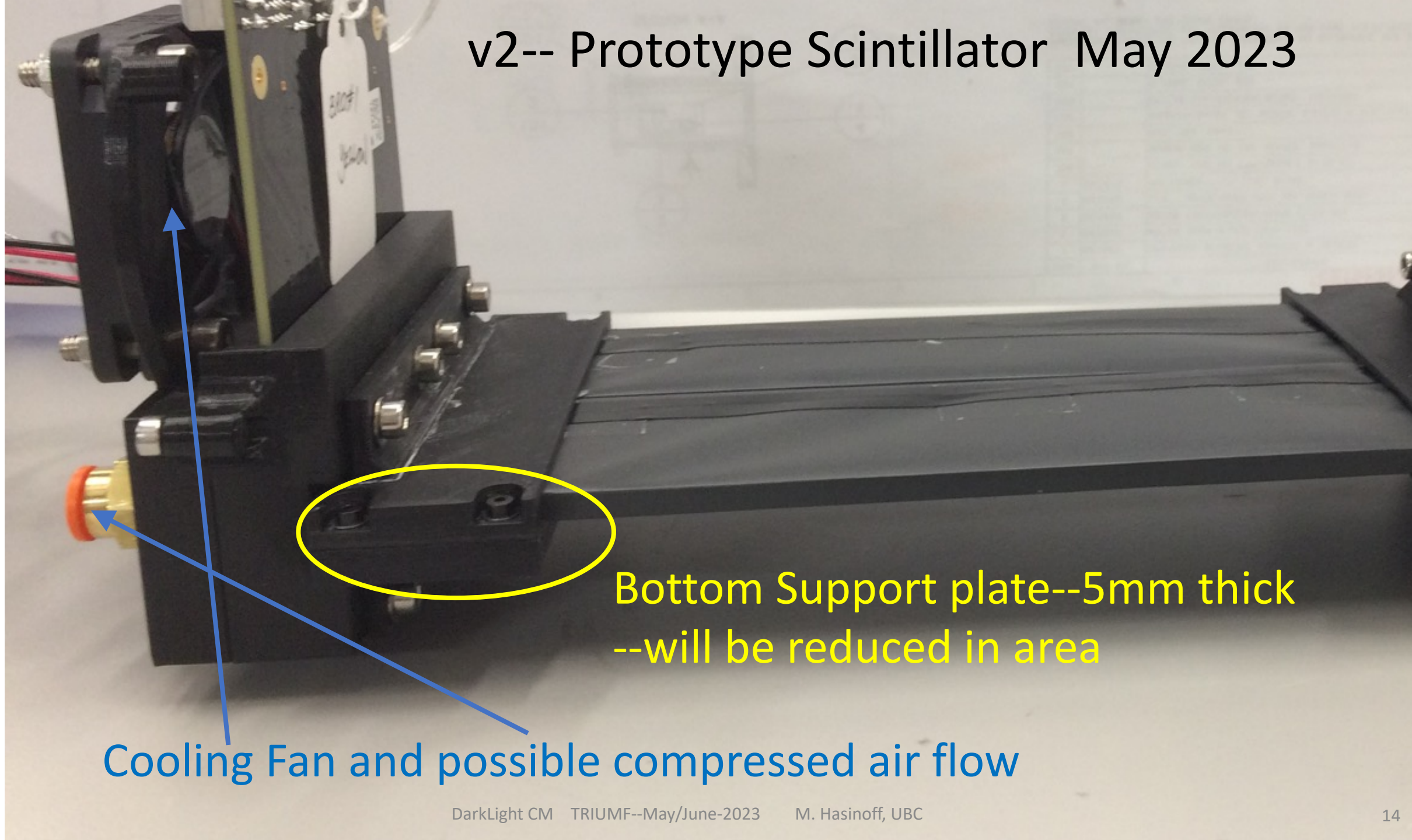
MCX output connectors
for Test-out &
pulser-in signals



v2-- Prototype Scintillator May 2023



v2-- Prototype Scintillator May 2023



Cooling Fan and possible compressed air flow

Bottom Support plate--5mm thick
--will be reduced in area