Integrated CMOS Sensor Development for Future Colliders with a US-Based Foundry

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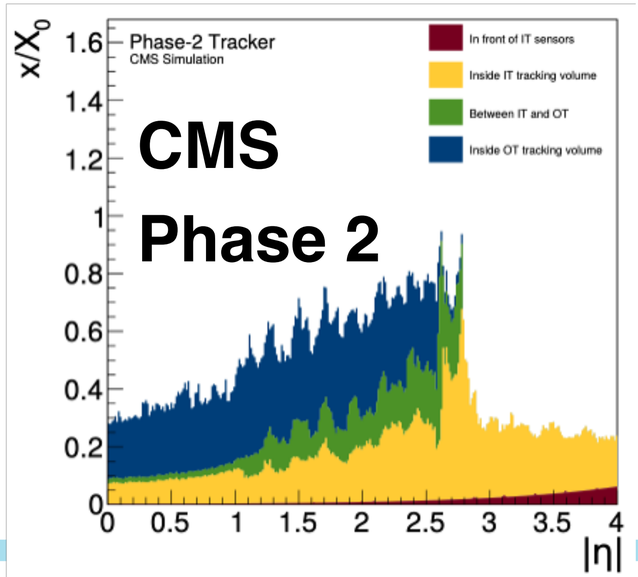
Ongoing Effort

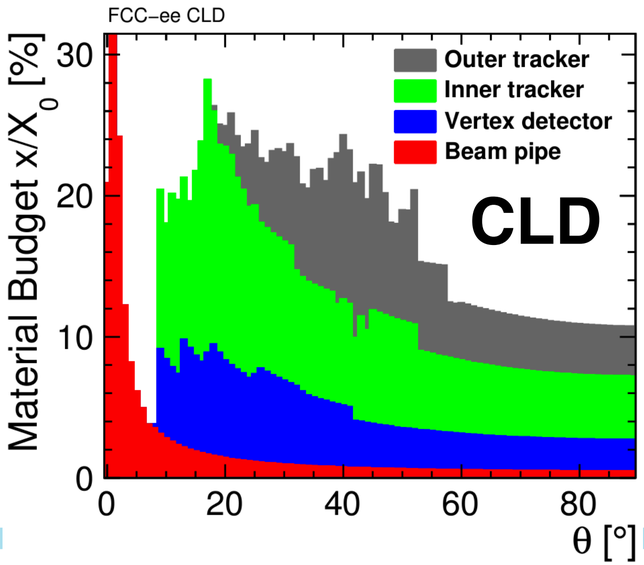
- PIs Involved:
  - Fermilab: A. Apresyan, M. Alyari, N. Bacchetta, D. Berry, T. England, F. Fahim, R. Lipton;
  - Purdue: M. Liu, M. Jones;
  - University of Chicago: K. Di Petrillo;
  - University of Illinois Chicago: C. Mills

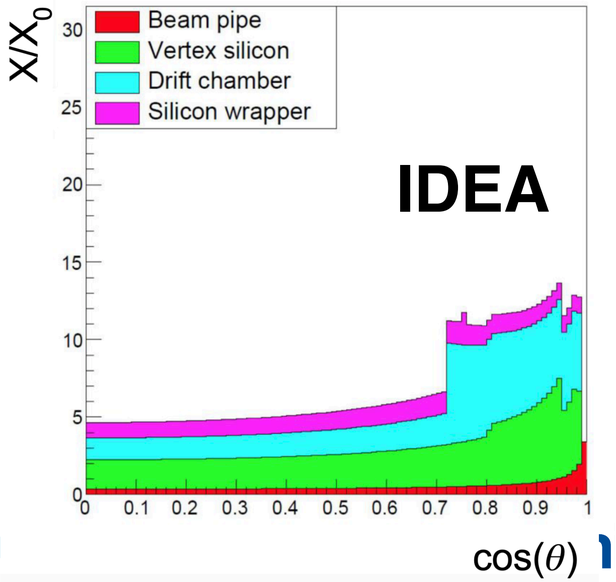
- Reference talks:
  - Past talk: **CPAD 2023**
  - FCC workshop: **A. Apresyan**,

Motivation

- Tracking system will play decisive role for FCCee physics goal
  - A **low mass tracker** is required to provide measurements with a low enough systematic error to match the tremendous accumulated statistics
- **Require a 5 μm (0.1 mrad) spatial (angular) resolution**
- Very low mass budget
  - Total tracking material budget <30% X0 (less than half of upgraded CMS tracker budget)
- Recent developments of low-mass, low-power and low-cost CMOS MAPS make this the preferred option for FCCee.



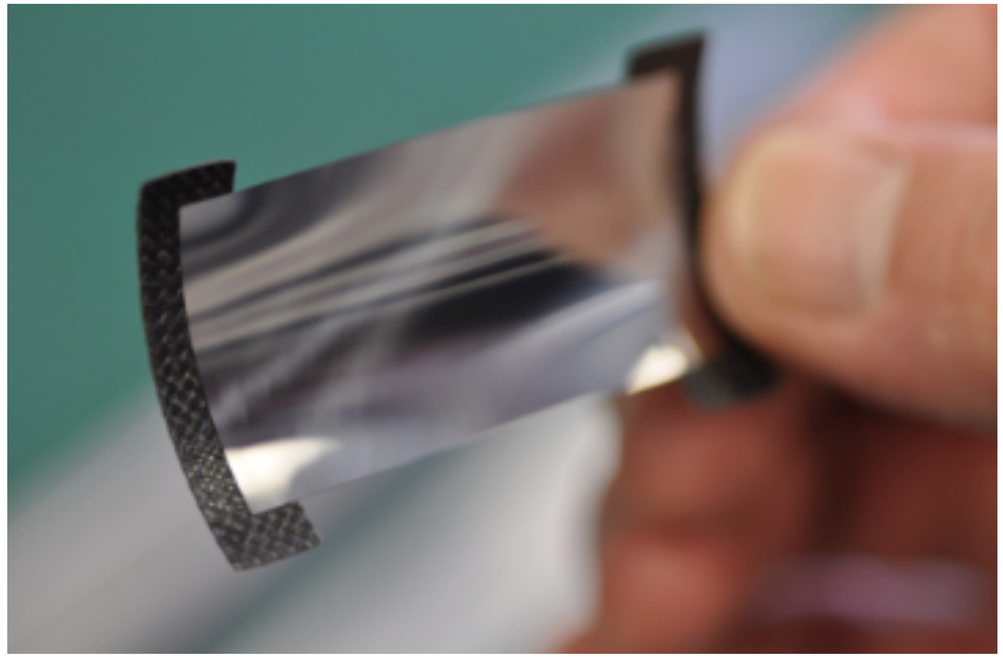


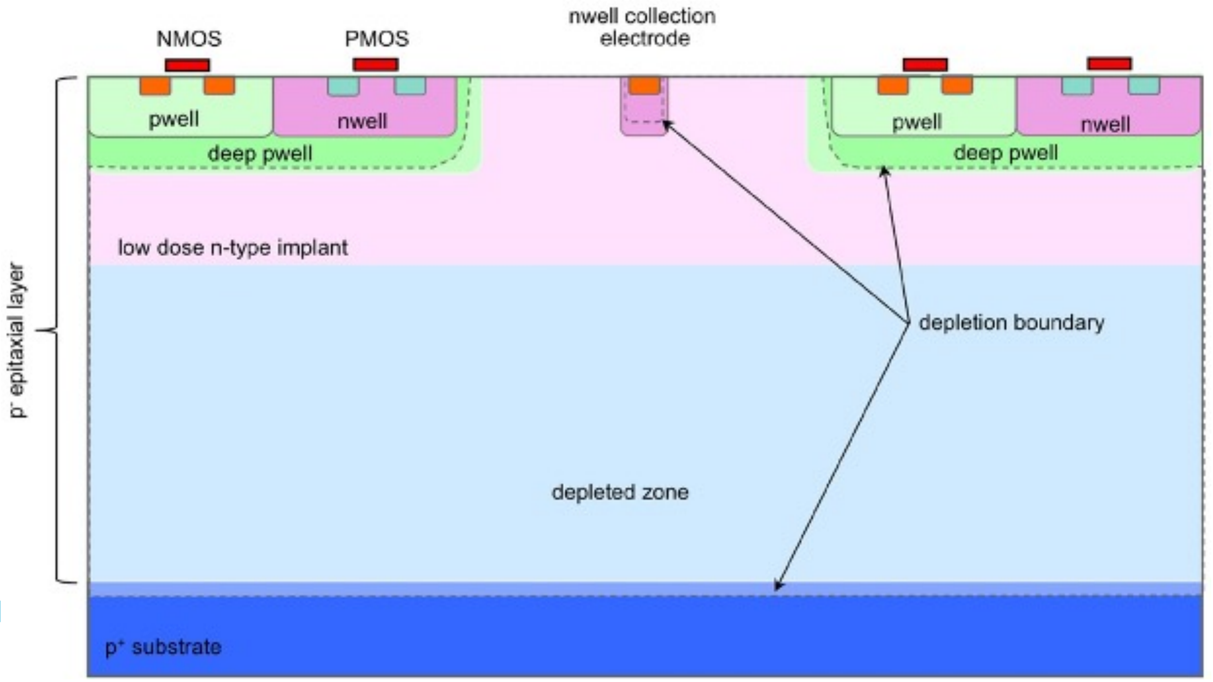


Sensor Proposal

- Advancing sensor technology
  - Monolithic Active Pixel Sensors (**MAPS**)
  - Low Gain Avalanche Diodes (**LGADs**)
  - Single Photon Avalanche Diodes (**SPADs**)
    - Critical components in trackers and calorimeters

- Fabricated in a standard CMOS process
  - Excellent spatial resolution (~5 μm)
  - Low-power consumptions (<40 mW/cm2)
  - Low mass (~0.05 X0)
  - Low cost for large volume fabrication

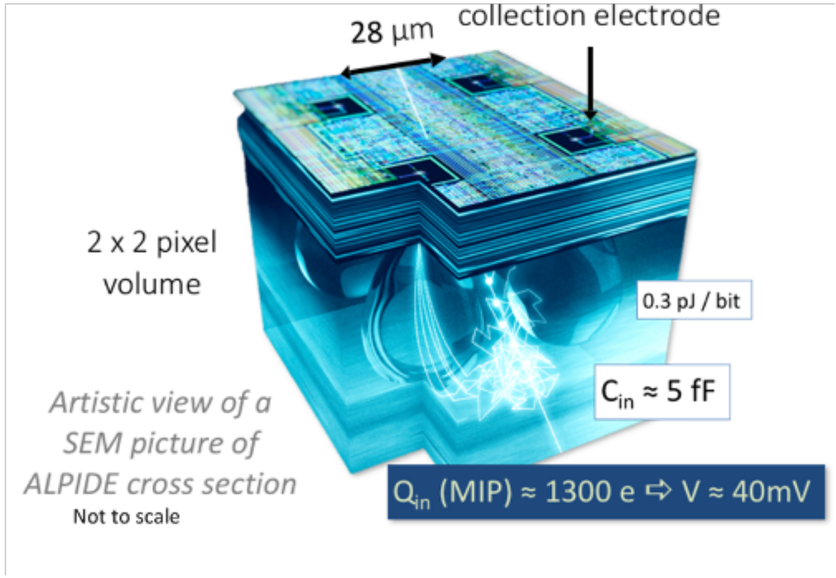




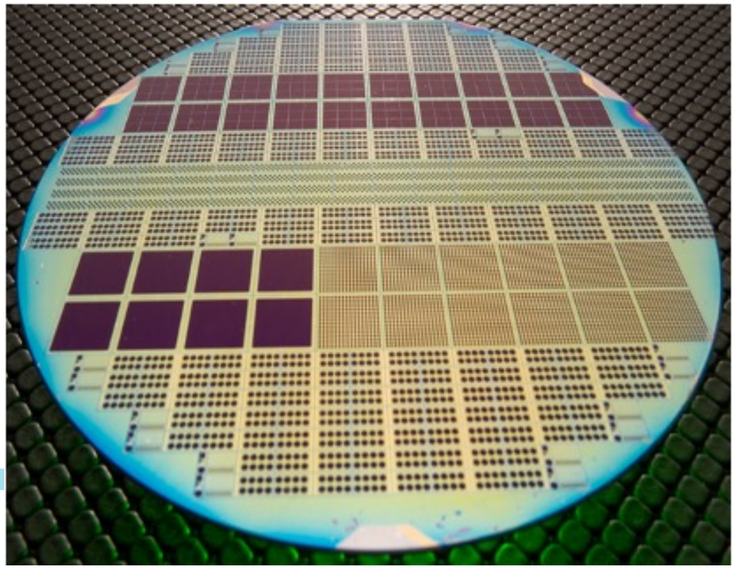
CMOS Sensors Production

- **GOALS**
  - US manufactured sensor capability for HEP experiments
  - Optimize the process towards HEP sensors
  - Co-design sensor and readout electronics
  - Broad adoption of development in community

- **HOW?**
  - **Fabricated on Skywater's 90 nm process**
    - Based out of Bloomington, Minnesota
  - Strong support from UC, UIC, Purdue, UIUC, Cornell, …
  - Engineering run with various designs
  - Testing of sensors at Fermilab and partners

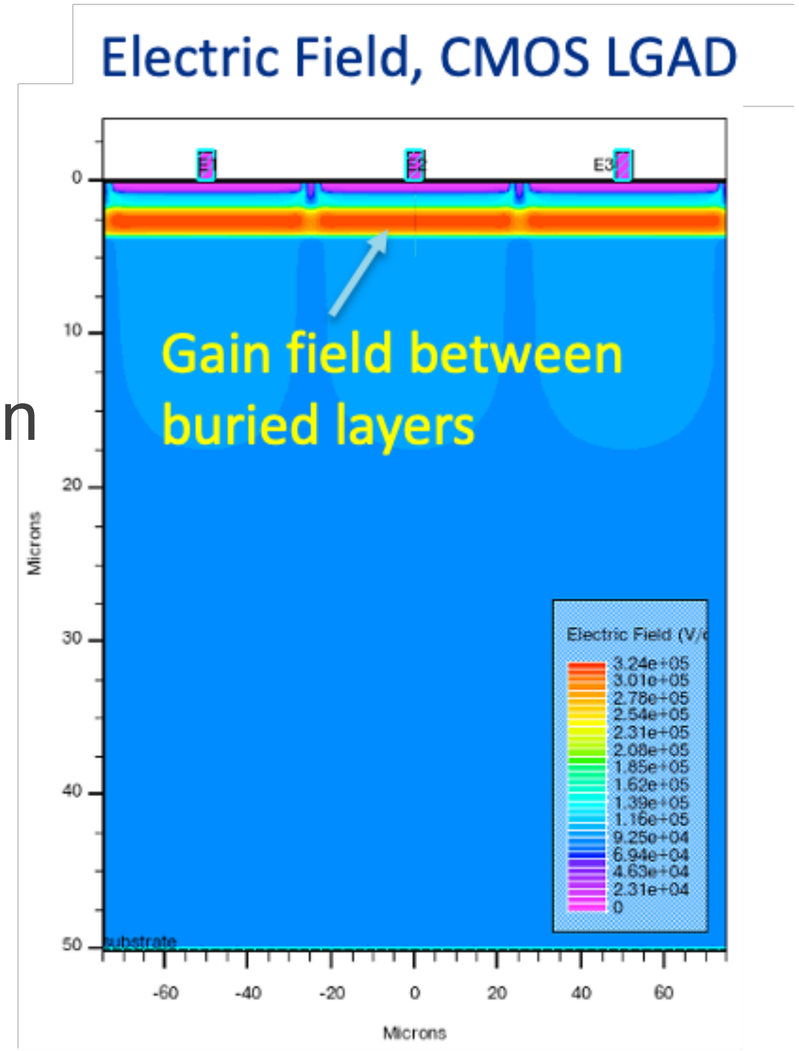


skywater
NASDAQ: SKYT

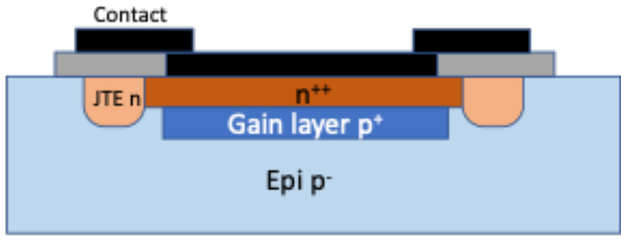


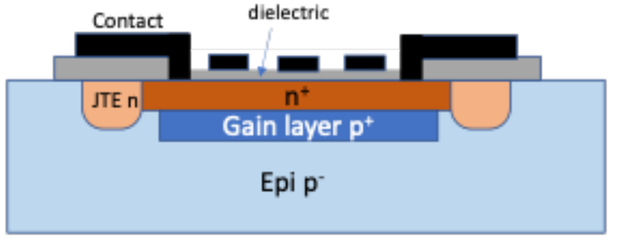
LGADs

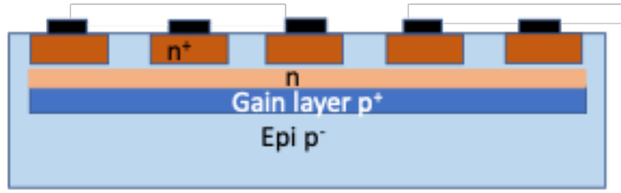
- Low Gain Avalanche Diodes
  - MAPS devices with linear gain
  - Deep buried junction to isolate gain field from CMOS wells
- High energy implants or graded epitaxy



LGAD Variants

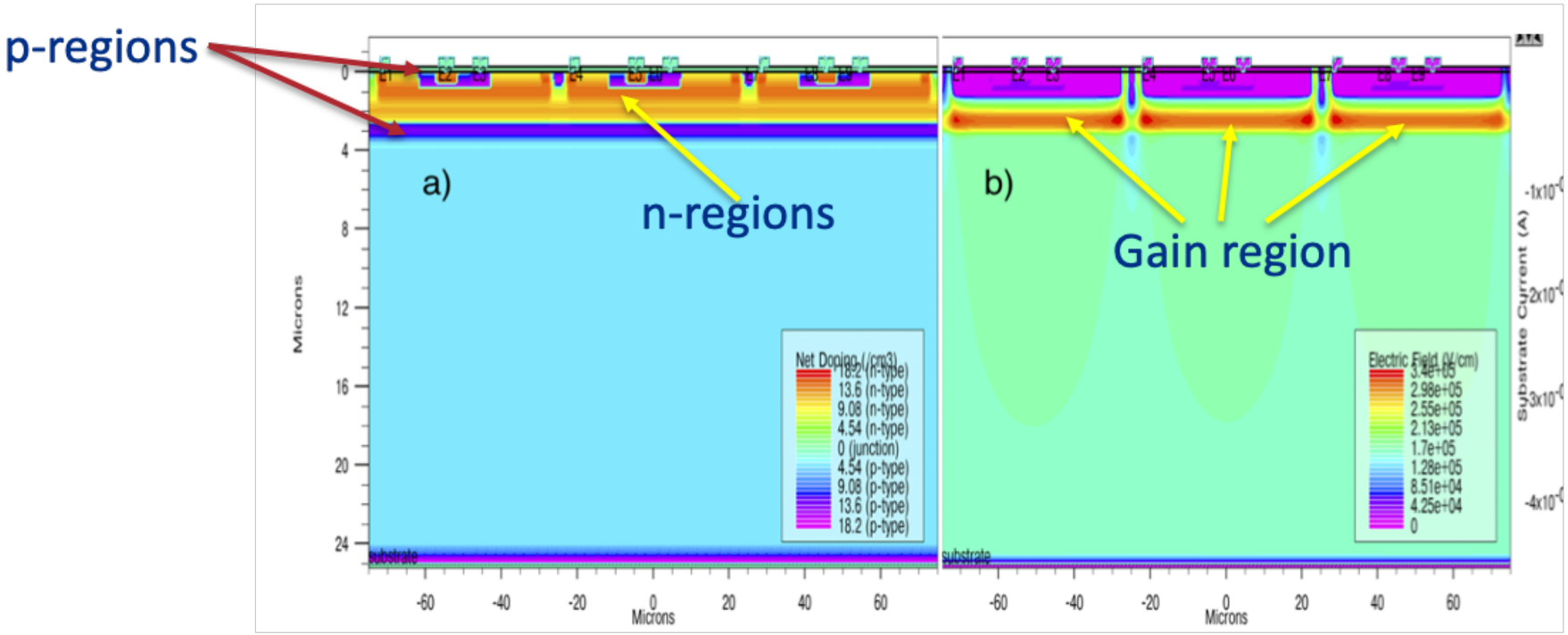






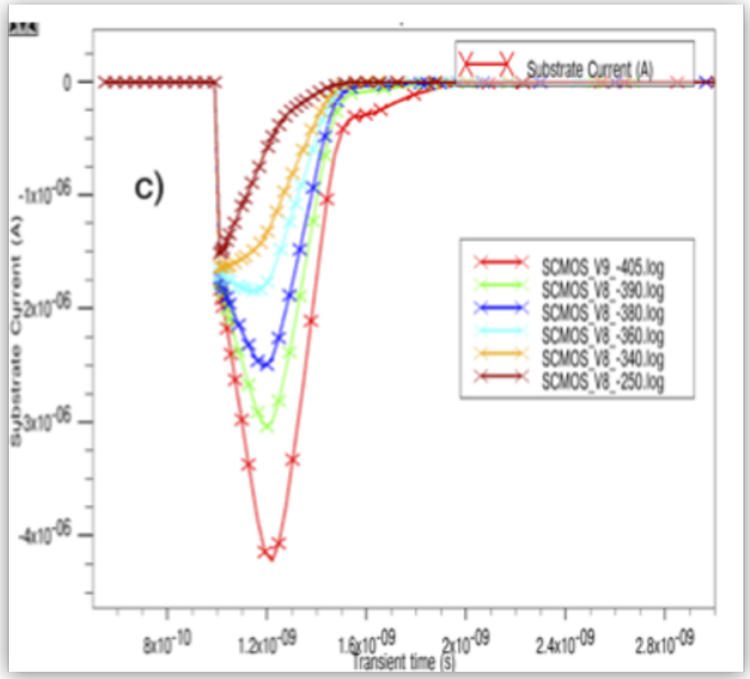
Simulations

- TCAD simulations were used to establish the feasibility of the proposed work, and we started discussions with SkyWater.
  - The initial TCAD studies for SkyWater CMOS are promising



Net doping density of the structure

Electric field profile



Summary

- Establish a US based CMOS manufacturing process
  - Target applications are FCCee and other HEP and NP experiments that require low-mass, high-speed, precise charged particle tracking.

- Lays the foundation of CMOS sensor manufacturing in the United States
  - A stepping stone for the domestic fabrication of the next generation of tracking sensors

- Integration with the ongoing international efforts within DRD3 and DRD5 efforts
  - Development of **tracker** and **calorimeter** designs for the **Higgs factories**

Backup

HEP CMOS Sensors vs CMOS Image Sensors (CIS)

- Although similar in concept HEP CMOS sensors differ from CIS devices
  - Charge generated in HEP sensors is distributed along a particle track → no need for a transparent entrance window. As much of this charge as possible should be collected.
  - Pixels can be large: 20 – 50 μm
  - The collection region should be fully depleted if possible. We aim for ~ ns charge collection.
  - The collection well contains complex circuitry: amps, discriminators, logic…
  - Fields near the n-well limit the applied bias due to breakdown to the epi. HVCMOS can be used extend the bias voltage. This effect can also be mitigated by additional deep implants.