DESIGN, PERFORMANCE AND FUTURE PROSPECTS FOR A VERTEX DETECTOR FOR FCC-EE

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2nd Annual U.S. Future Circular Collider Workshop
MIT
25 – 27 March 2024

Outline

- **Mid-Term feasibility study Vertex layout with carbon fibre supports**
  - Inner and Outer vertex mechanical description
  - Study of the services routings
- **Toward material budget reduction – a lightweight layout ALICE ITS3 inspired**
  - Proposed layout of a low-mass curved inner vertex layout
- **Conclusions**

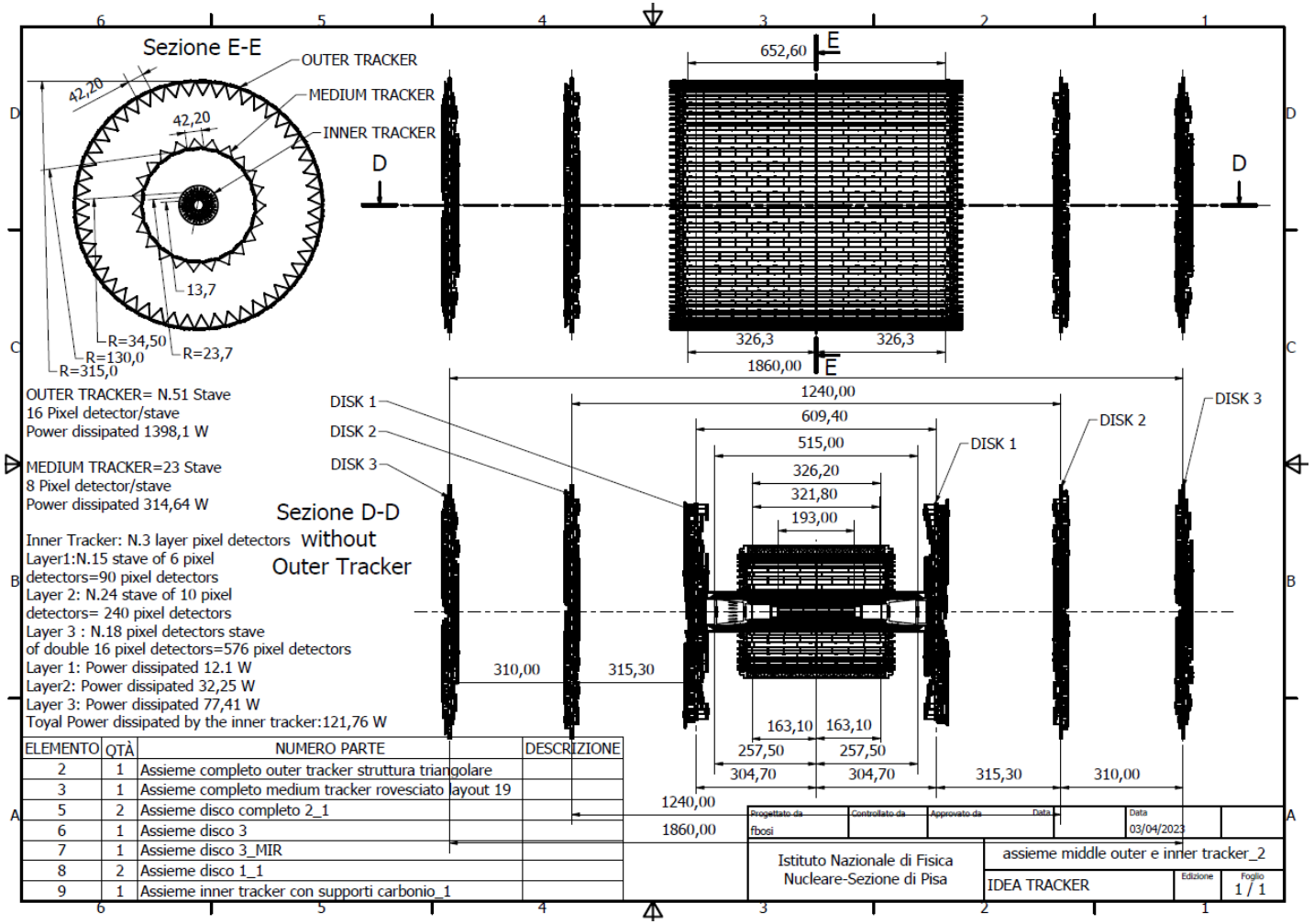
Requirements

Interaction region detectors must be integrated with the beam pipe

- The vertex detector innermost radius should profit of the small beam pipe diameter (2 cm) and should cover $|cos\theta| < 0.99$
- Must not interefere with the Luminosity Calorimeter (clearance of ~120 mrad)
- The mounting of the vertex tracker must be done inside the support tube
- Minimize the radiation length
- Minimize power dissipation
- While simulations are progressing, requirements are getting more clear and stringent: a global optimization is required and the design parameters (for instance pitch) will change

Mid-term feasibility study vertex detector layout

(disclaimer: mean focus on integration in MDI – no optimisation wrt initial IDEA concept)



Outer vertex tracker:

Modules of $50 \times 150\ \mu m^2$ pixel size

- Intermediate barrel at 13 cm radius (improved reconstruction for $p_T > 40$ MeV tracks)
- Outer barrel at 31.5 cm radius
- 3 disks per side

Inner Vertex detector:

Modules of $25 \times 25\ \mu m^2$ pixel size *

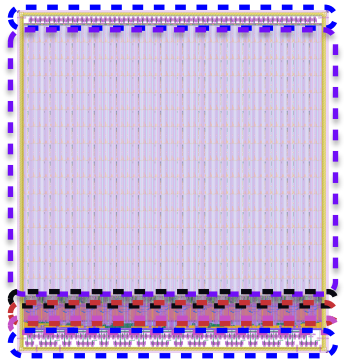
3 barrel layers at
- 13.7, 22.7 and 34.8 mm radius

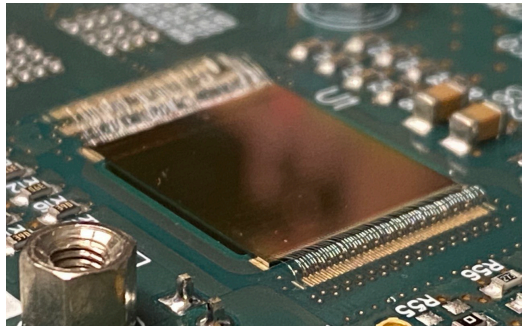
(*) the pitch is the one of ARCADIA

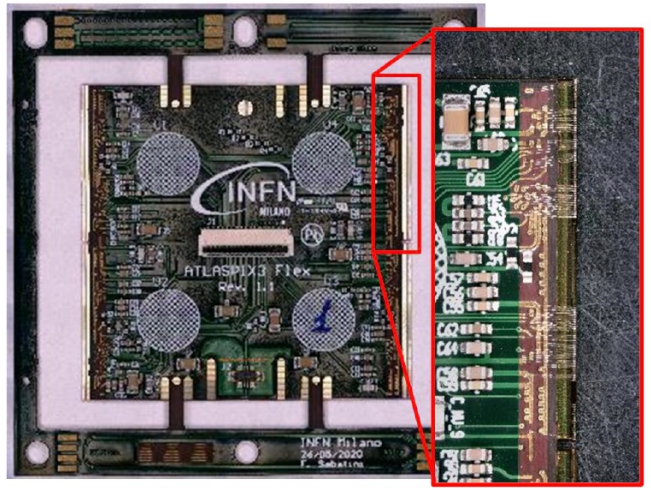
Sensors technology and dimensions

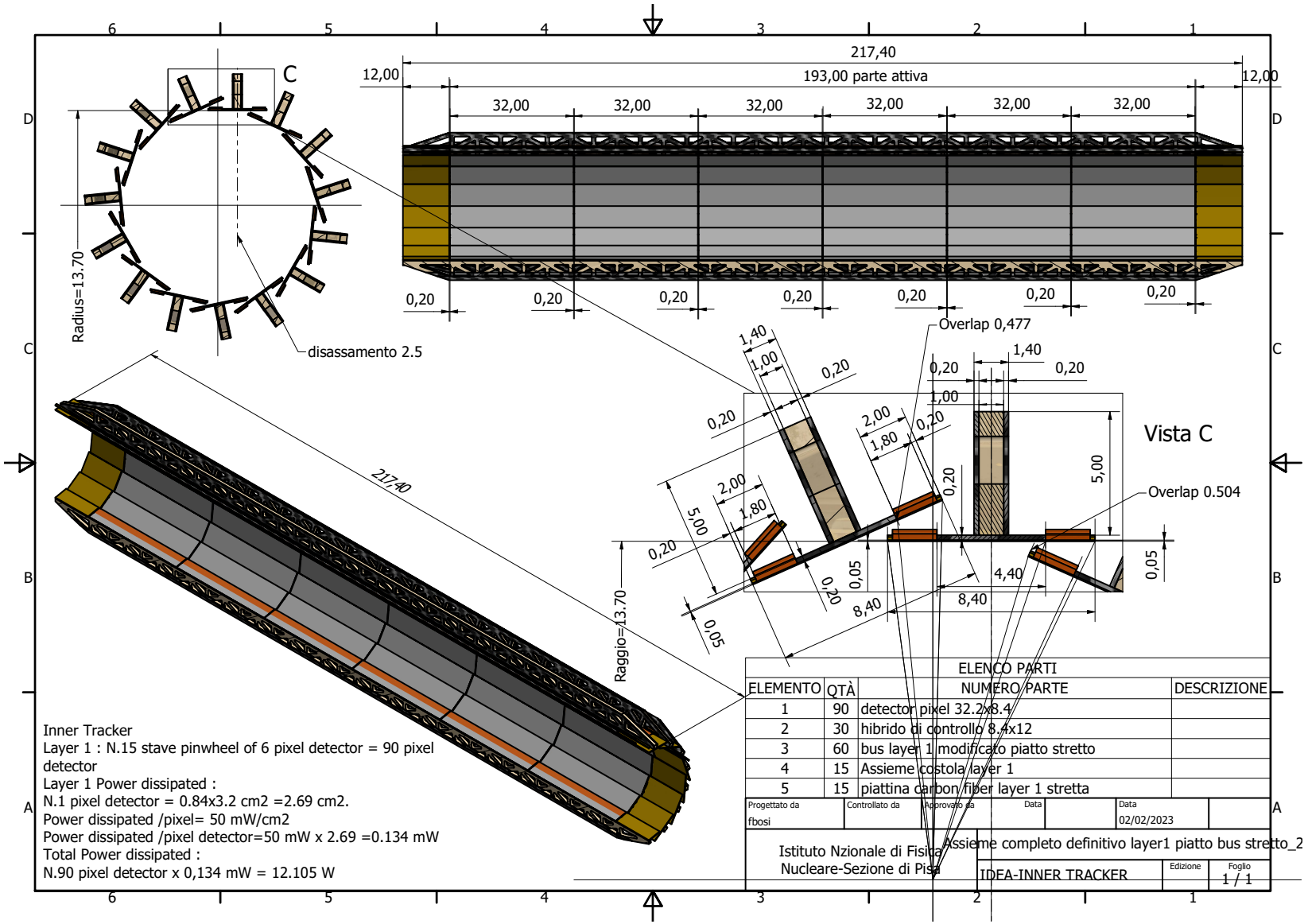
Depleted Monolithic Active Pixel Detectors

- **Inner Vertex (inspired to ARCADIA):**
  - Lfoundry 110 nm process
  - *50 μm thick, 25 μm x 25 μm*
  - Module dimensions: $8.4\times32\ mm^2$
  - Power density $50\ mW/cm^2$ (core $30\ mW/cm^2$)
  - **Current at 100 MHz/cm²**
- **Outer Vertex and disks (inspired to ATLASPIX3)**
  - TSI 180 nm process
  - *50 μm thick (50 μm x 150 μm)*
  - Module dimensions: $42.2\times40.6\ mm^2$
  - Power density: assume $100\ mW/cm^2$
  - **Up to 1.28 Gb/s downlink**









Layer 1

15 overlapping staves of 6 modules each

Overlap to allow alignment ~500 μm

Pinwheel geometry: all modules at the same (smallest) radius

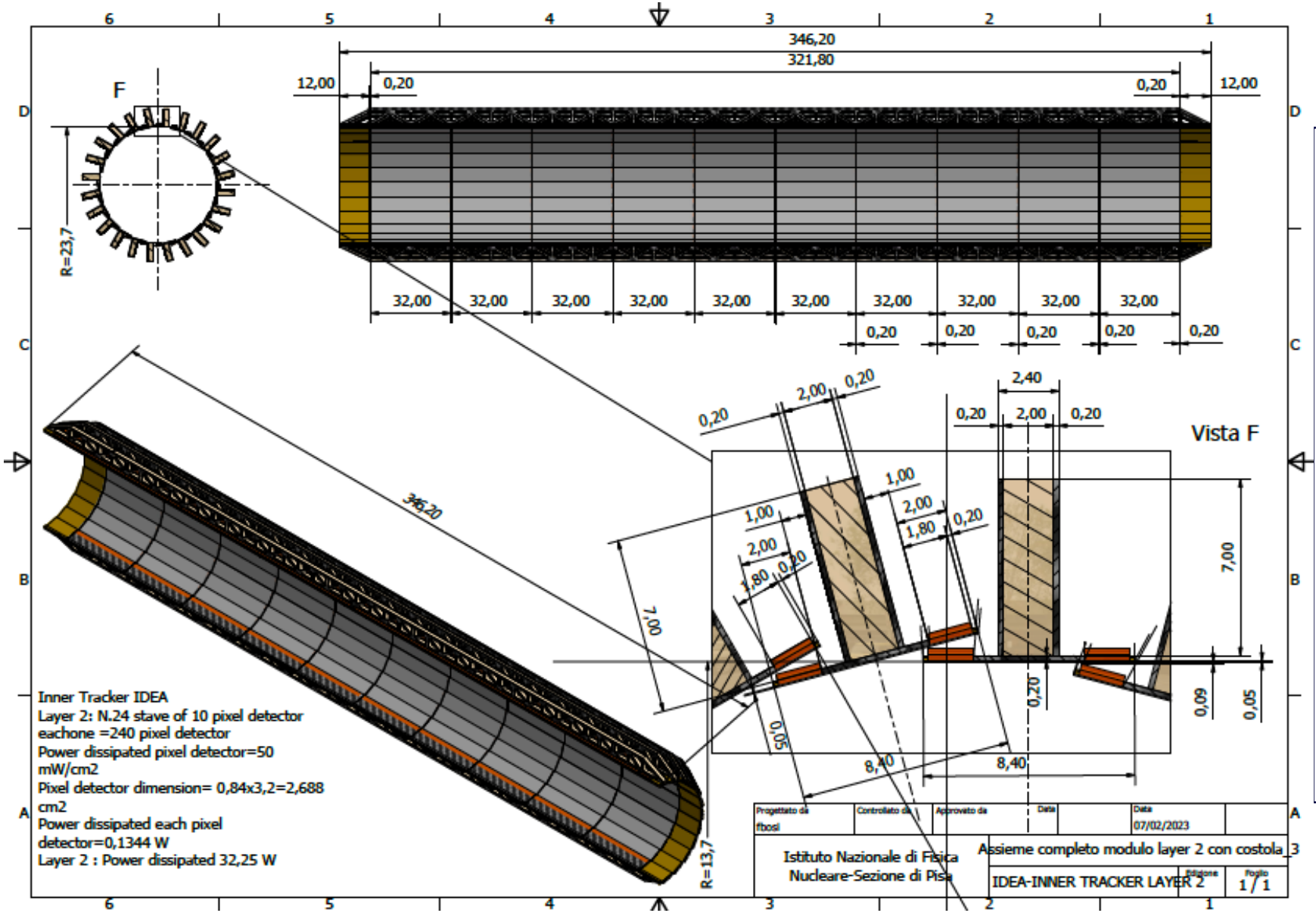
Power budget ~12 W

Total weight ~22 grams

Total thickness 0.25% X_0

Silicon: 0.053% X_0

Power and readout bus: 0.056% X_0



Layer 2

24 overlapping staves of 10 modules each

Pinwheel geometry

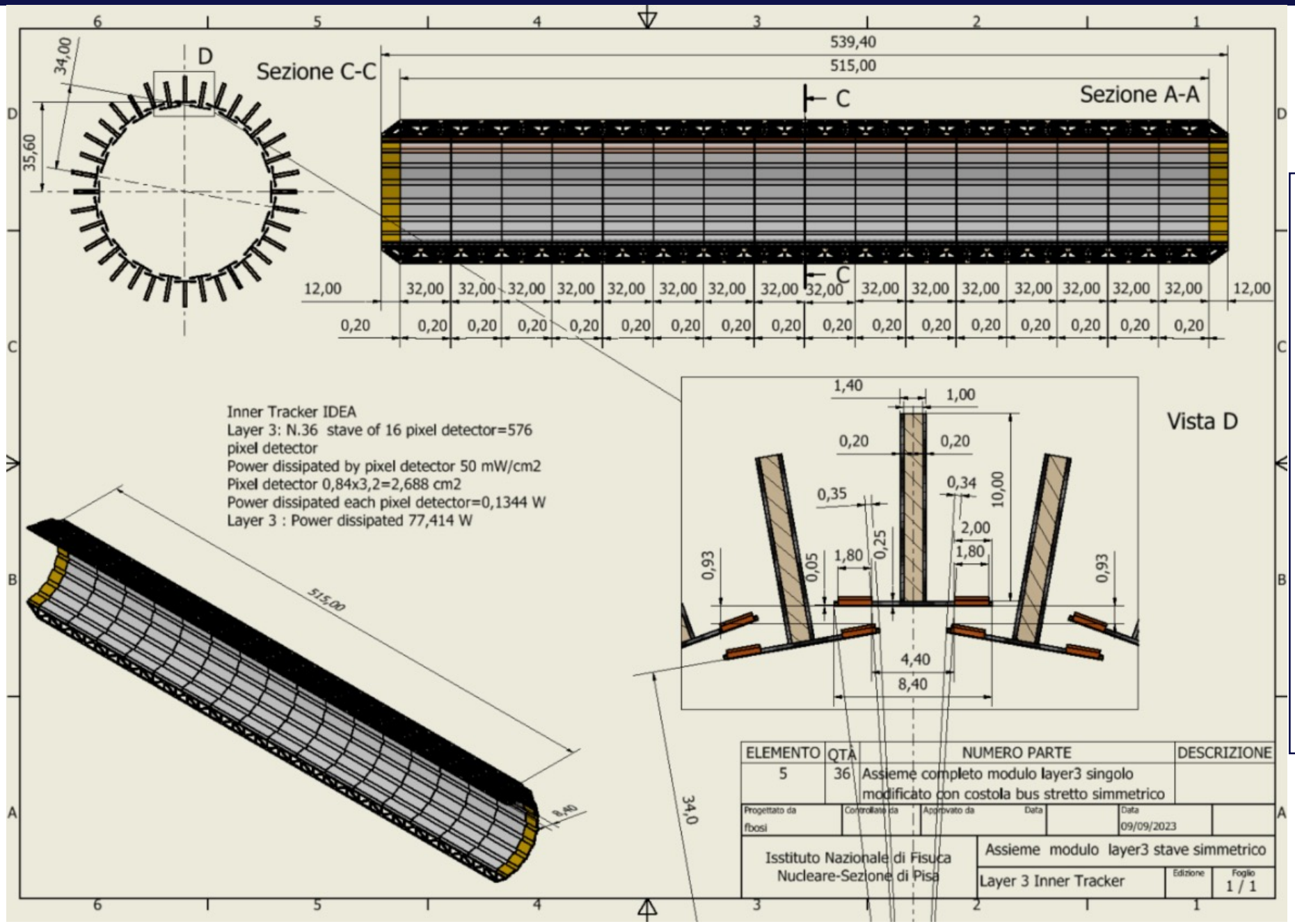
Counter-rotated wrt layer 1 to mitigate charge-asymmetry effects in track reconstruction

Power budget

~32 W

Total weight ~63 grams

Total thickness 0.25% X_0



Layer 3

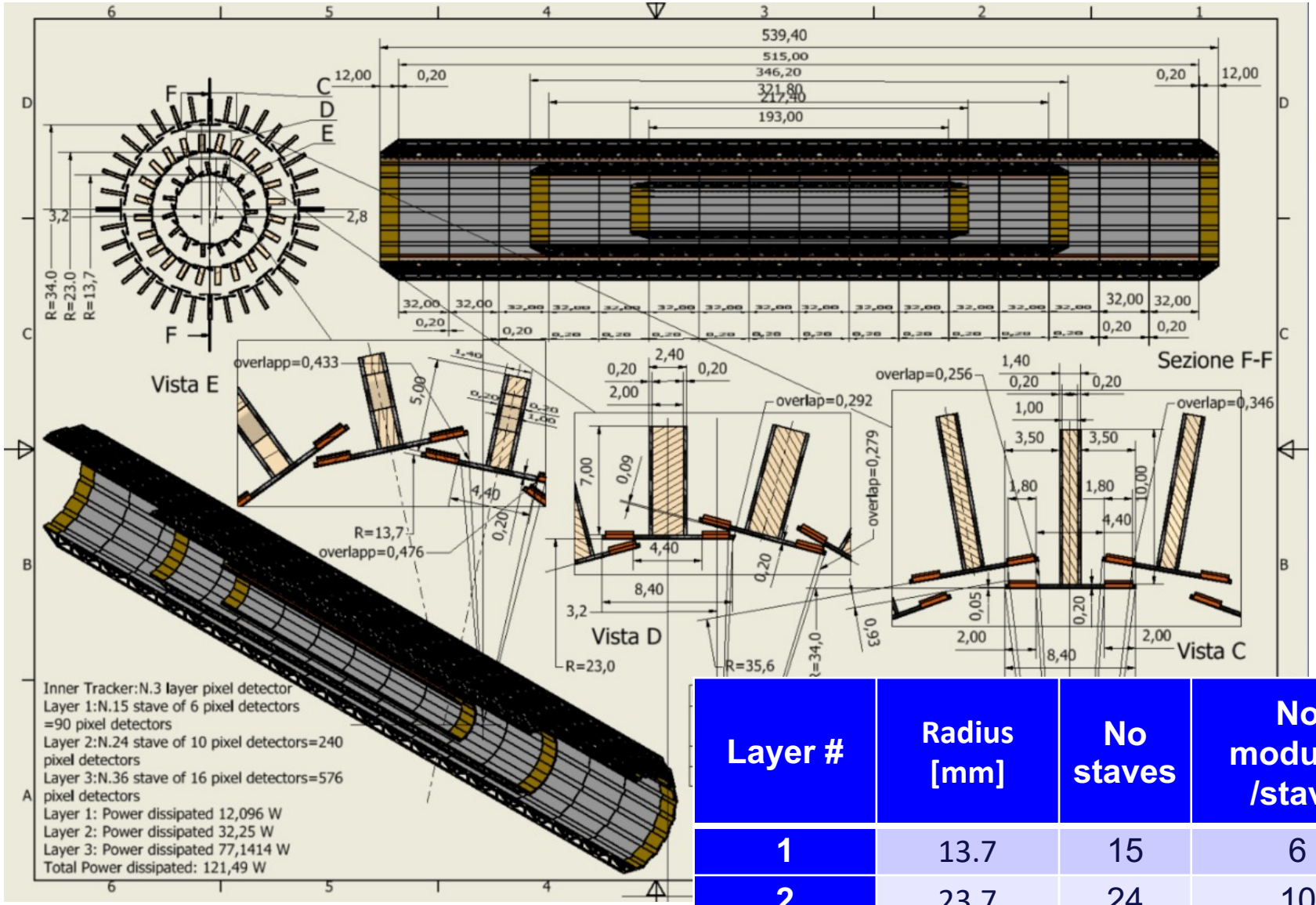
36 staves of 16 modules each

Lampshade geometry.
Charge symmetric track reconstruction

Total weight ~150 grams

Total thickness 0.25% X_0

Power budget
~77 W



Total thickness per layer 0.25% X/X0

Carbon Fibre ~60 %

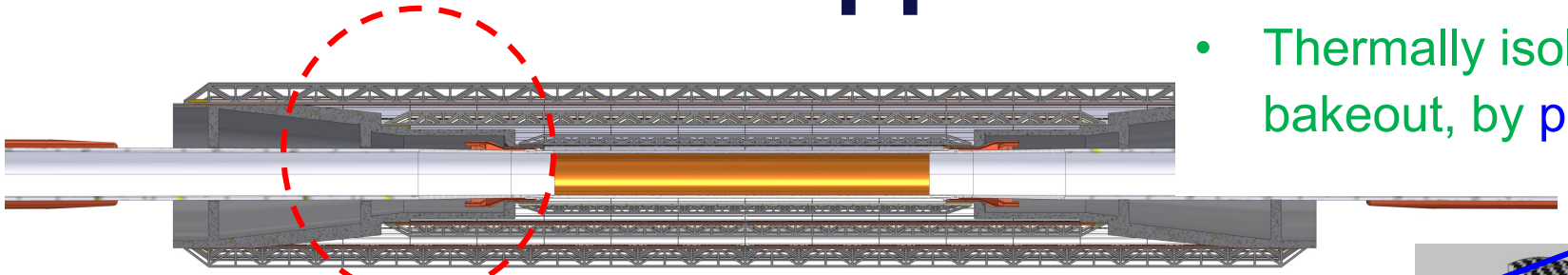
Silicon: ~20%

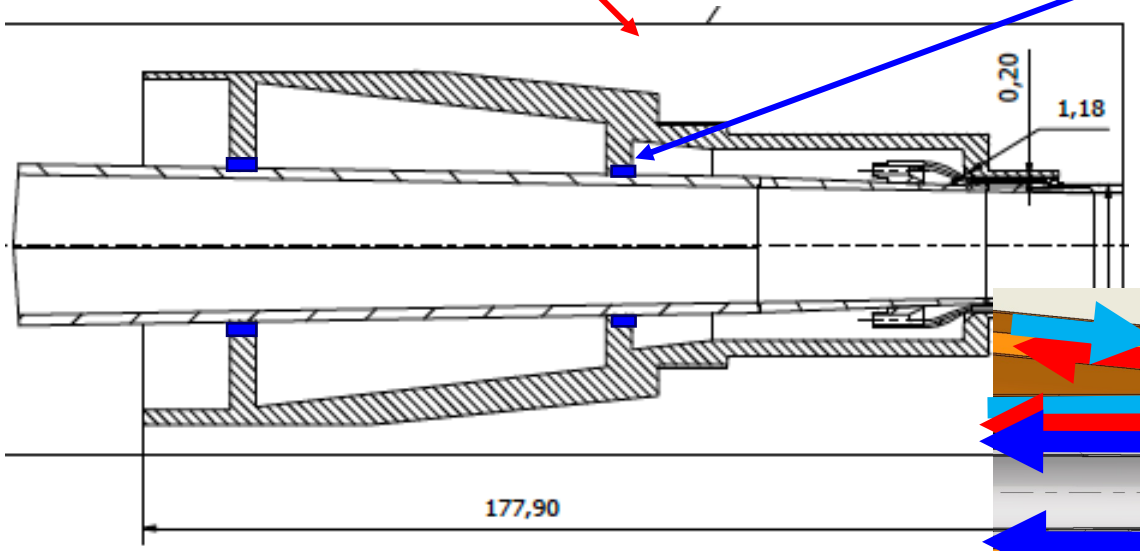
Power and readout bus: ~20%

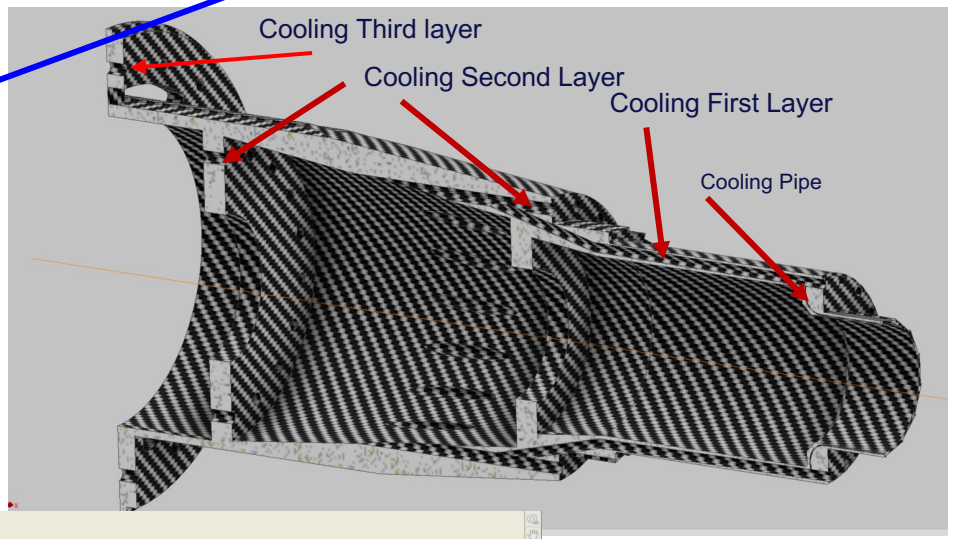
Layer #	Radius [mm]	No staves	No modules /stave	Total Length [mm]	Active Area [cm^2]	Power [W]
1	13.7	15	6	217.40	241.92	12
2	23.7	24	10	346.20	645.12	32
3	34 & 35.60	36	16	539.40	1548.29	77

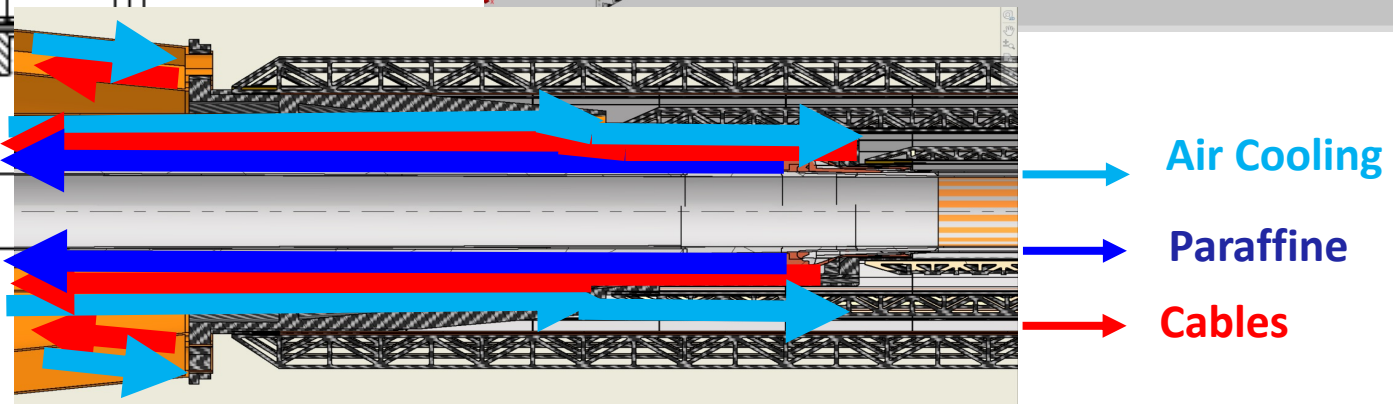
Inner Vertex support

- Anchored to the conical chamber
- Air cooled
- Thermally isolated from the beam pipe during bakeout, by peek supports

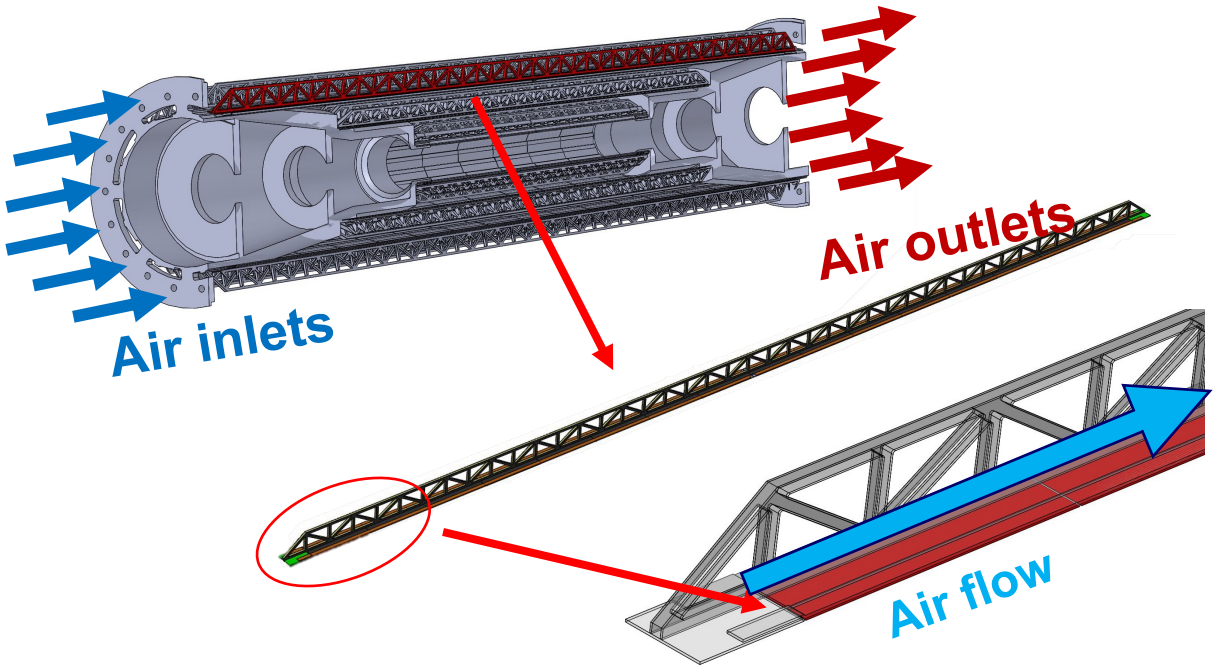


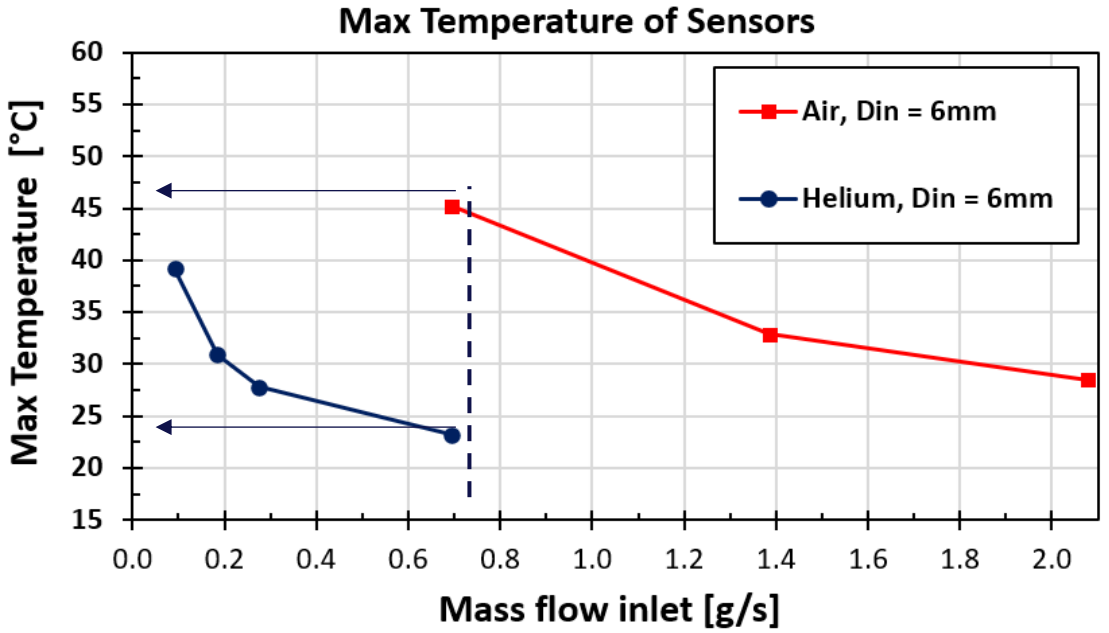




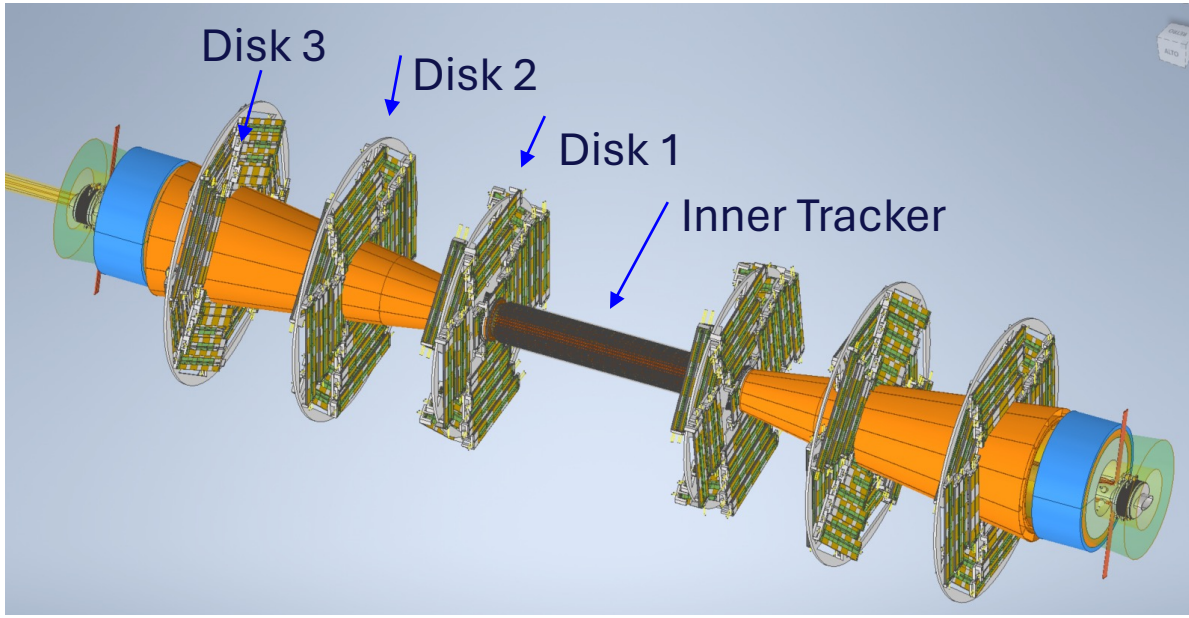


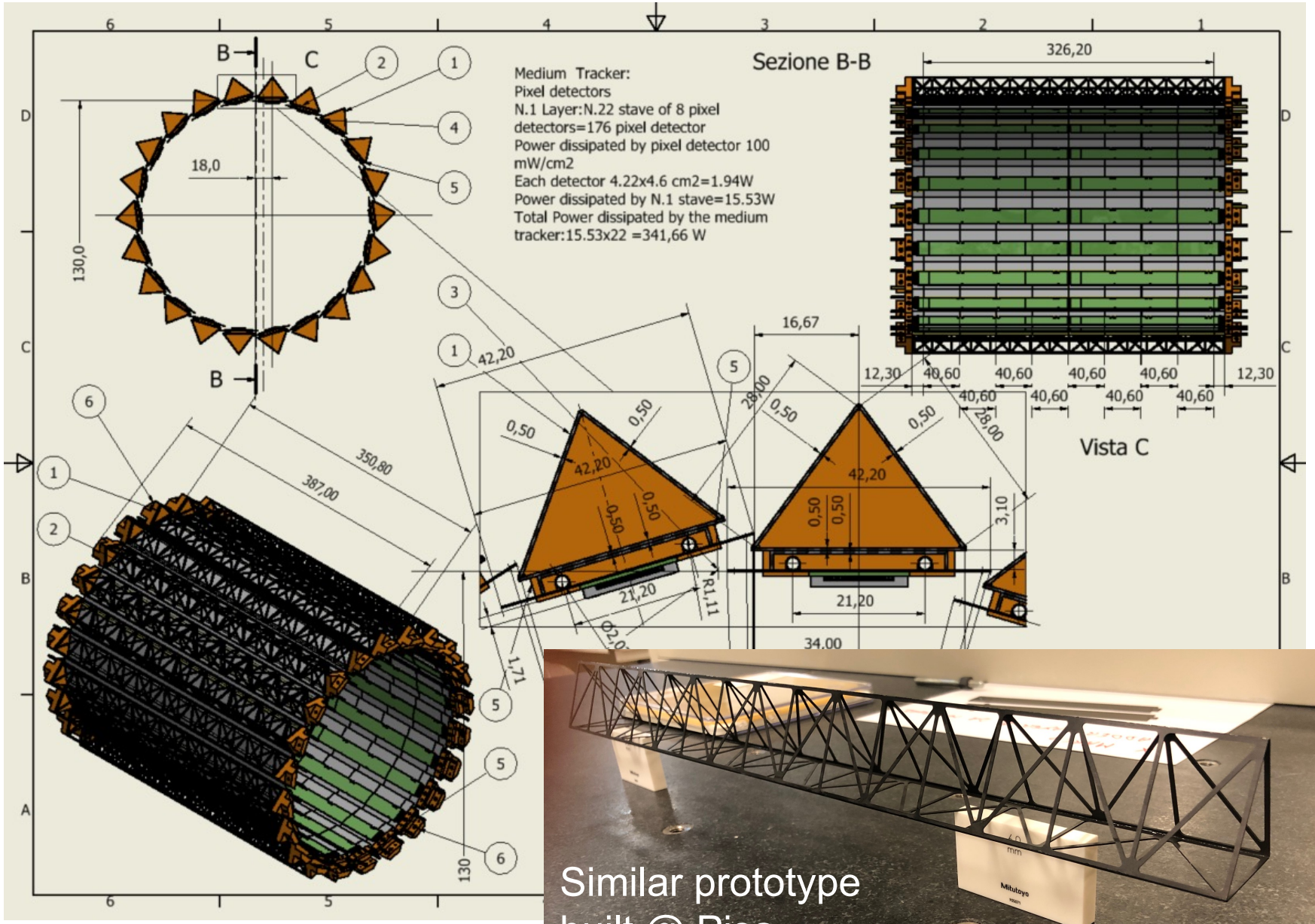
Air cooling (simulations)





- Cooling with air/He flow along the detector.
  - Air temperature: T_{air} = 15°C
  - Max sensor temp on layer 3 (hottest one) ~25/30 °C with He/Air.
  - Vibrations studies ongoing





Middle Barrel
At 13 cm radius

22 staves of 8 modules each.

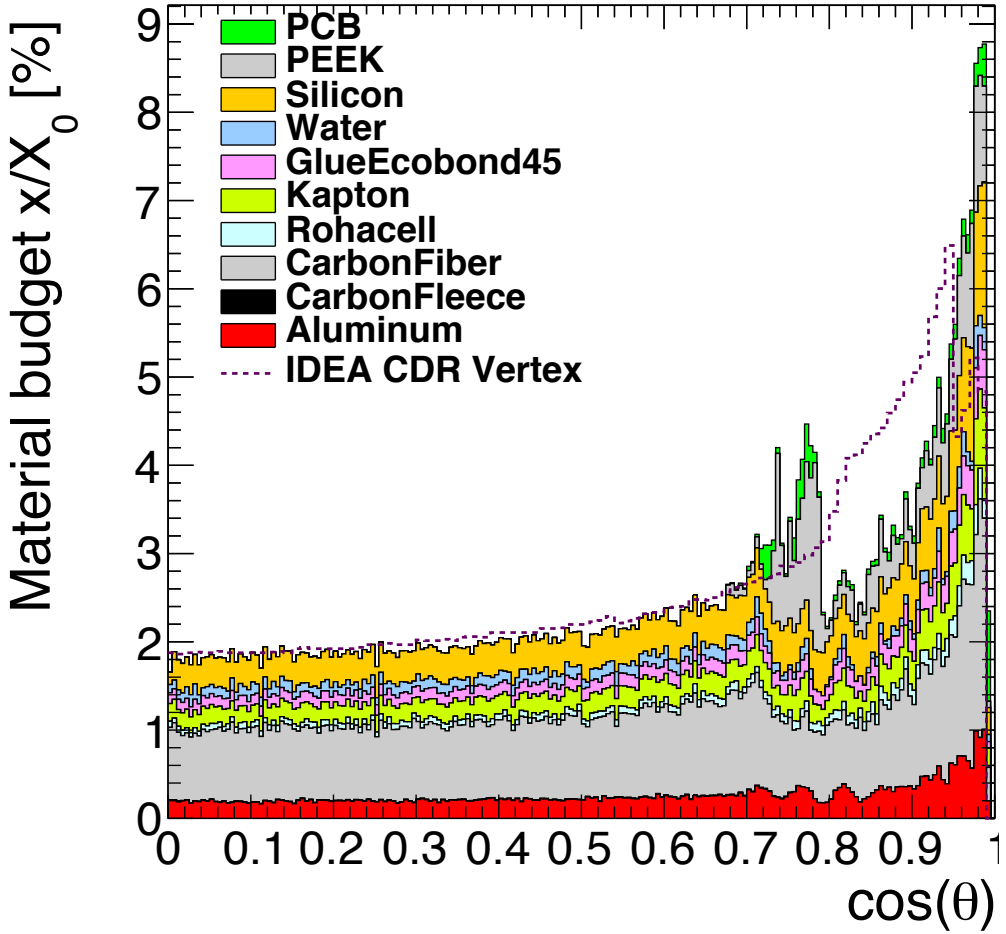
Lightweight reticular support structure (ALICE/Belle-II like)

Readout chips either side
Power budget
~342 W

Total weight ~1 kg
Water cooled (2 pipes of 2 mm diameter)

Outer barrel is similar but longer (see backup)

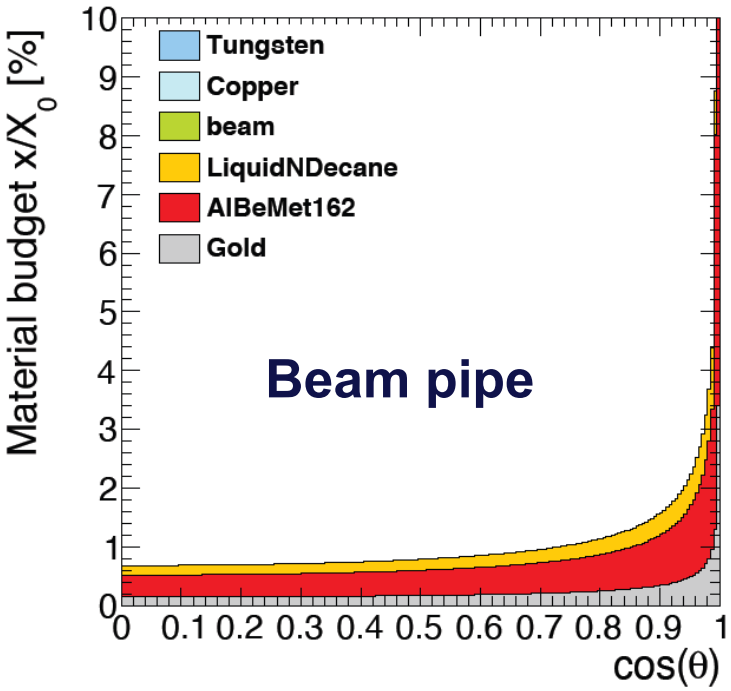
Simulated material budget

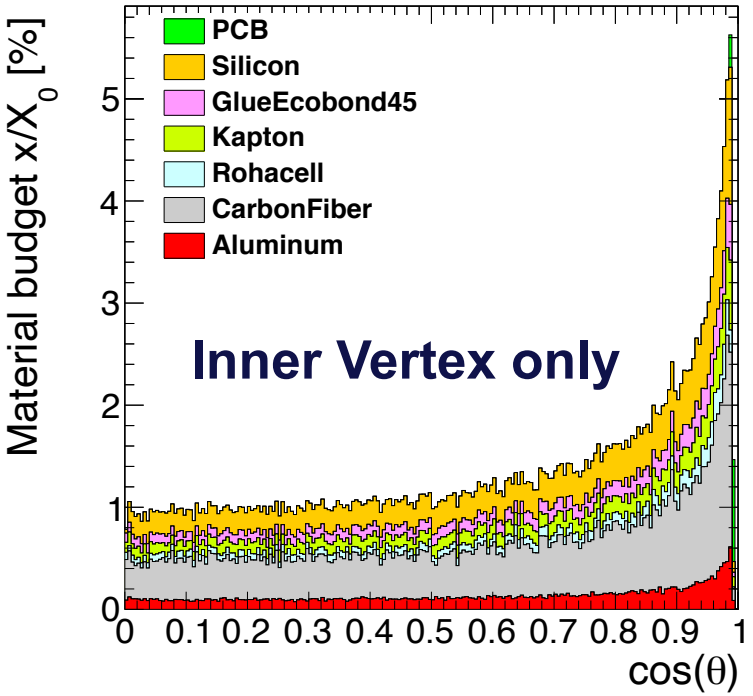


In agreement with CAD estimates

Smaller X/X_0 wrt IDEA CDR estimates even including power and readout cables in the sensitive region

Silicon only ~15% of the total



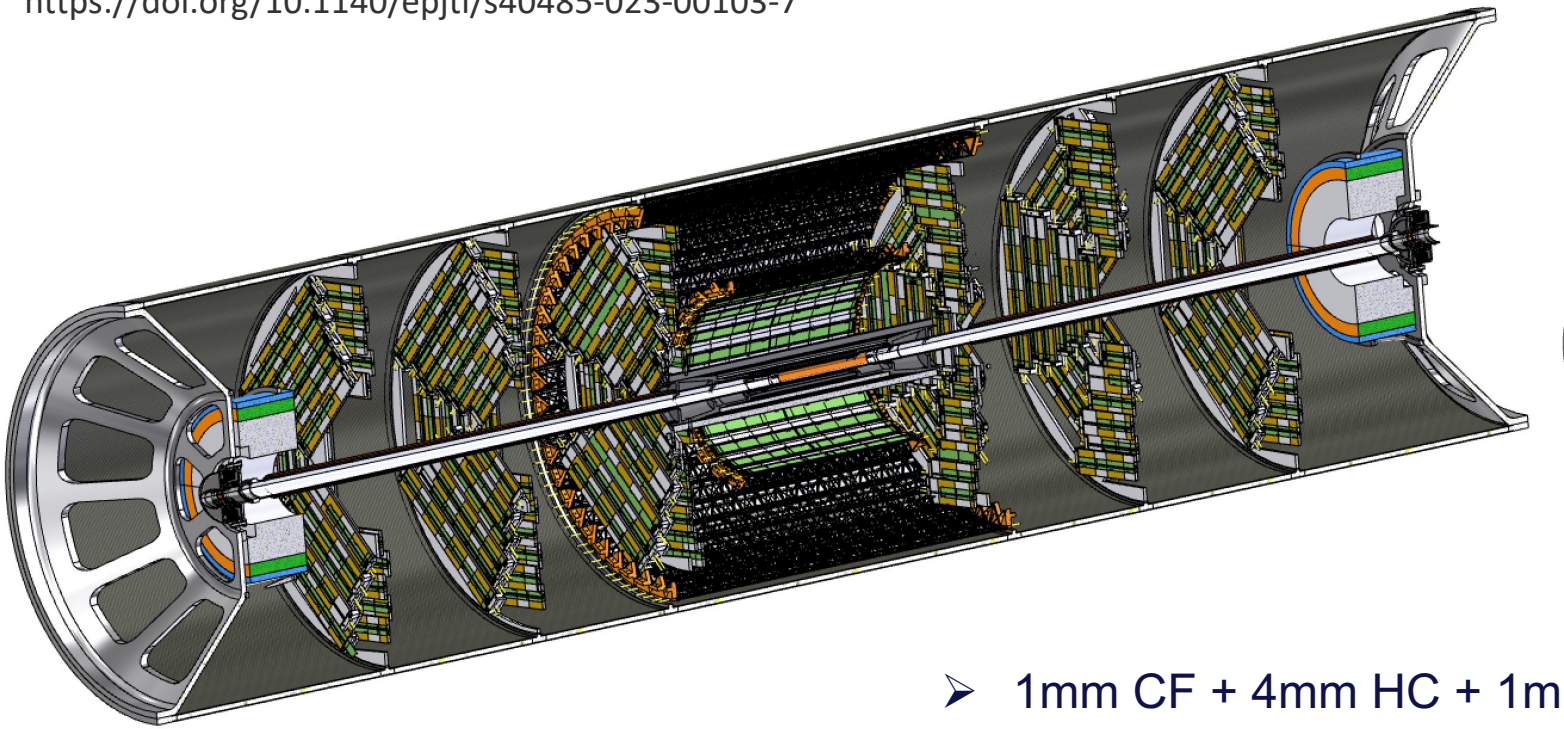


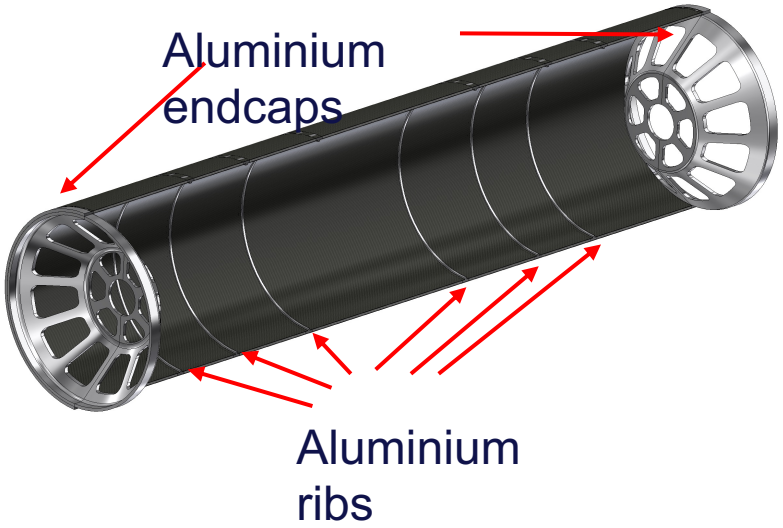
Support cylinder

All elements in the interaction region (Vertex and LumiCal) are mounted rigidly on a support cylinder that guarantees mechanical stability and alignment

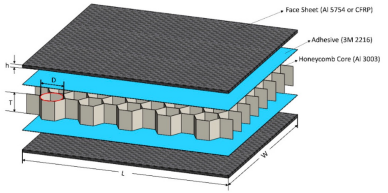
- Once the structure is assembled it is slided inside the rest of the detector

M. Boscolo, F. Palla, F. Fransesini, F. Bosi and S. Lauciani, Mechanical model for the FCC-ee MDI, *EPJ Techn Instrum* **10**, 16 (2023).
https://doi.org/10.1140/epjti/s40485-023-00103-7





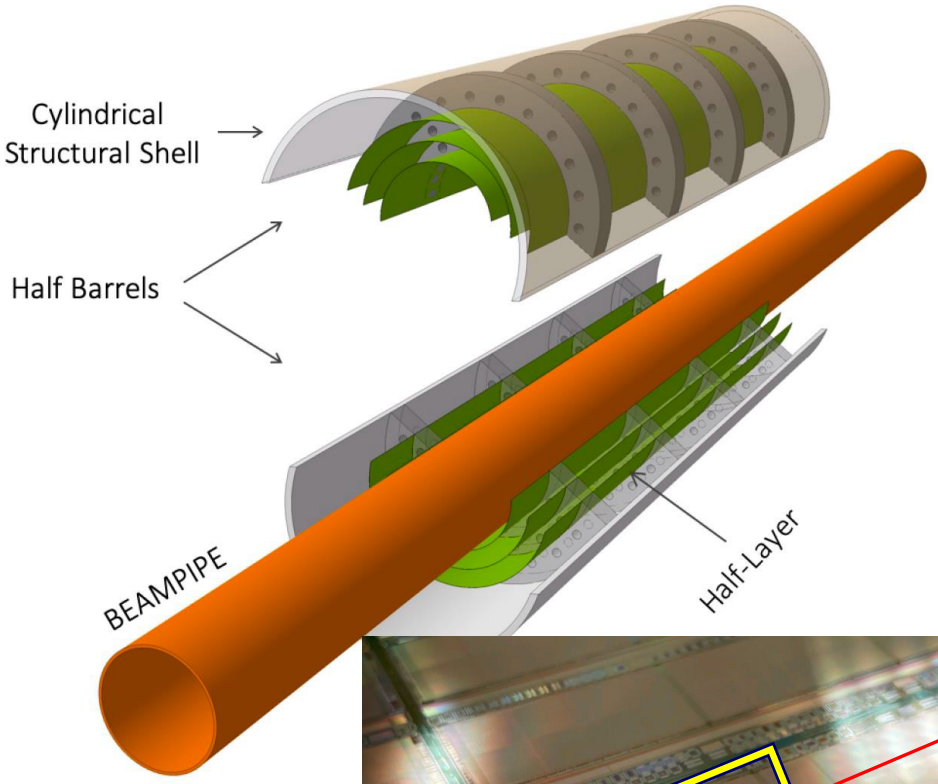
➢ 1mm CF + 4mm HC + 1mm CF

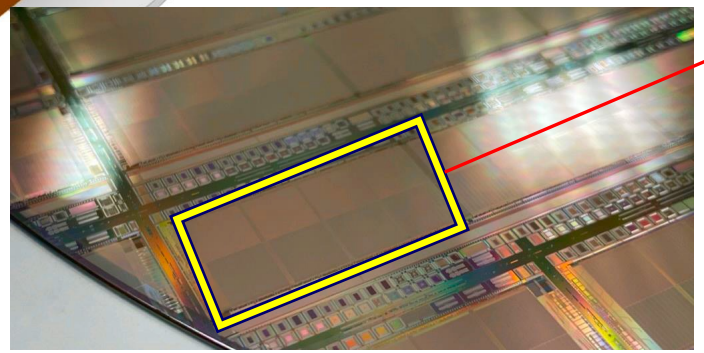


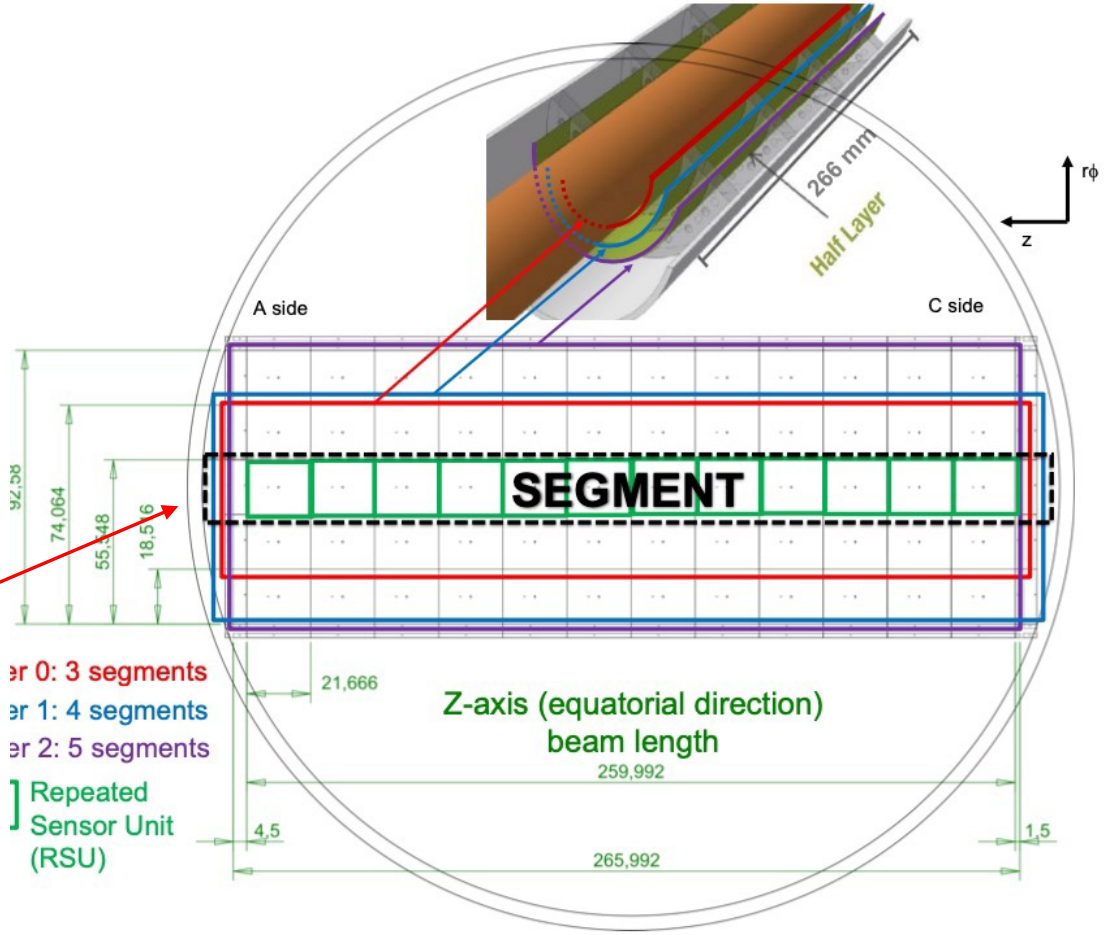
Data rates issues *(see F. Bedeschi talk at 7th FCC Workshop)*

- **Largest data rates occur at the Z energy**
- **Expected data rates per BX/module [cluster size 5]**
  - From machine backgrounds (Incoherent pair creation – safety factor of 3) ~ 19 hits/BX/module
  - From collisions (200 kHz) ~ average ~<1 hit/BX/module
- **Inner layer ~400 MHz/cm^2 → ~25 Gb/s per module**
  - might be reduced if cluster size is only 2 – as measured for many MAPS
  - *ALICE3 hit rate ~100 MHz/cm^2 (pixel size 10μm x 10μm)*
  - 2nd layer ~10x less data volume
- **Triggered readout**: for 200 kHz the data bandwidth per module, rate is only 150 Mb/s
  - Impact on physics?

- **All these depend on pixel pitch, thickness, R/O architecture, bias voltage.**
  - For a review see M. Winter talk at March 11 meeting







Proposed layout using an ALICE ITS3 inspired design

(~0.05 % X/X_0 material budget per layer – 5 times less than the Mid-Term one)

After fruitful discussions with ***C. Gargiulo, A. Junique, G. Aglieri Rinella, W. Snoeys***

ELECTRICAL UNITS

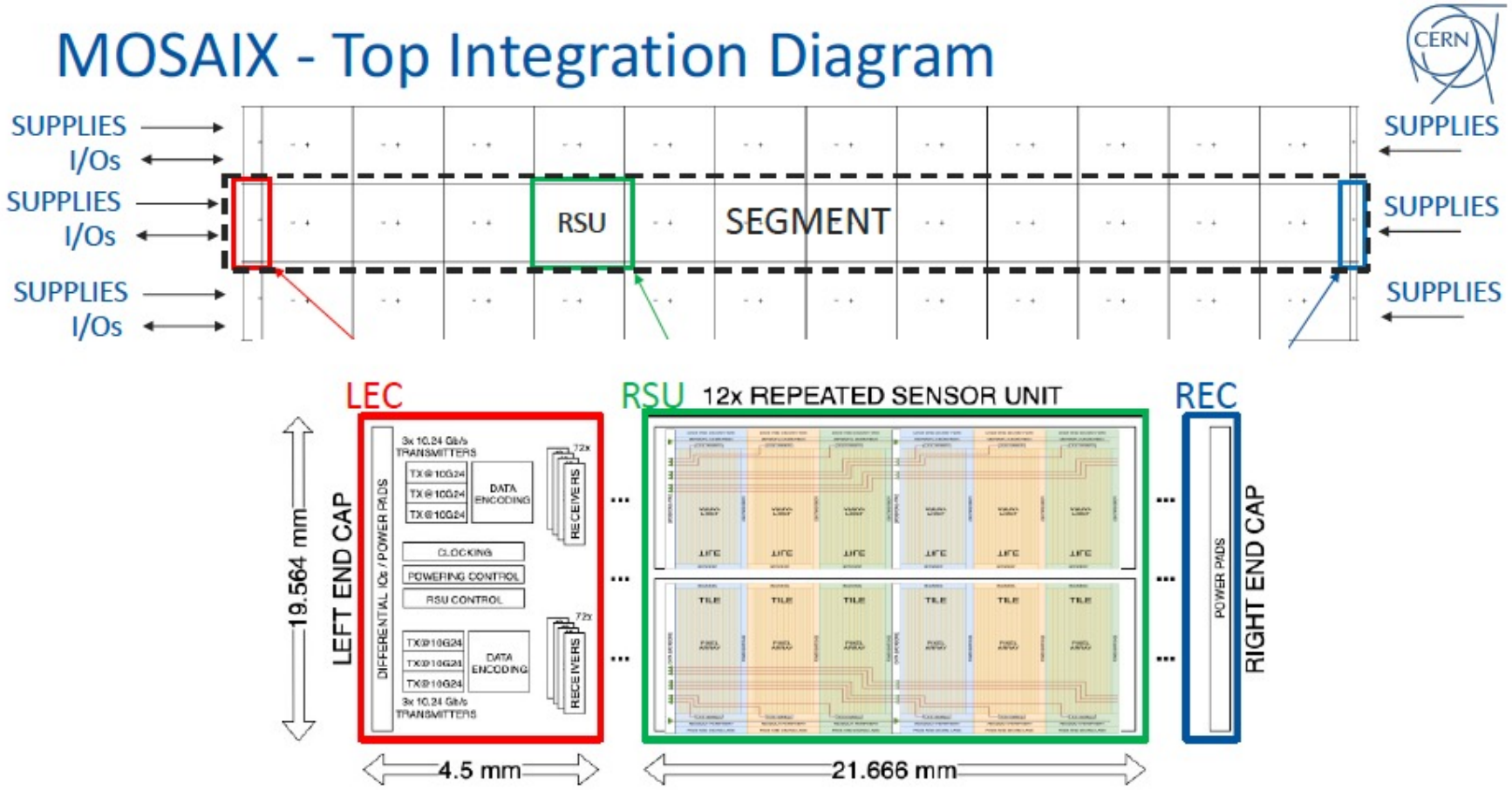


Figure 3.34: Block diagram of the sensor segment.

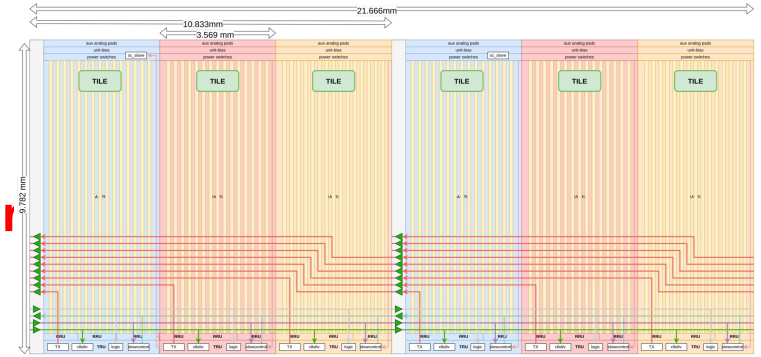
2023/12/01 | WP1.2 Plenary | ER2 Stitched Sensor Design 7

A column driven approach reaches higher bandwidth, but needs low power consumption

Issues

ALICE smaller radius will be 18 mm (beam pipe 16 mm)

- To demonstrate bent MAPS 13.7 mm radius works electrically – mechanically is OK



Active pixels <95% of covered area (chip service zones)

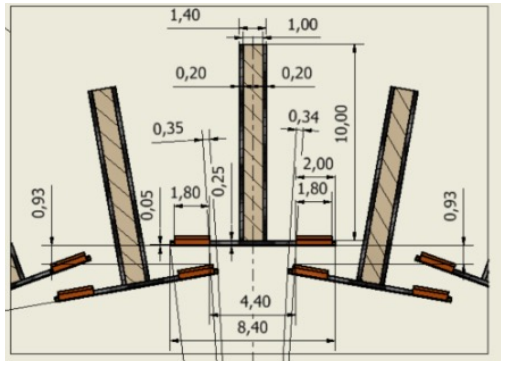
- Which impact has on physics?

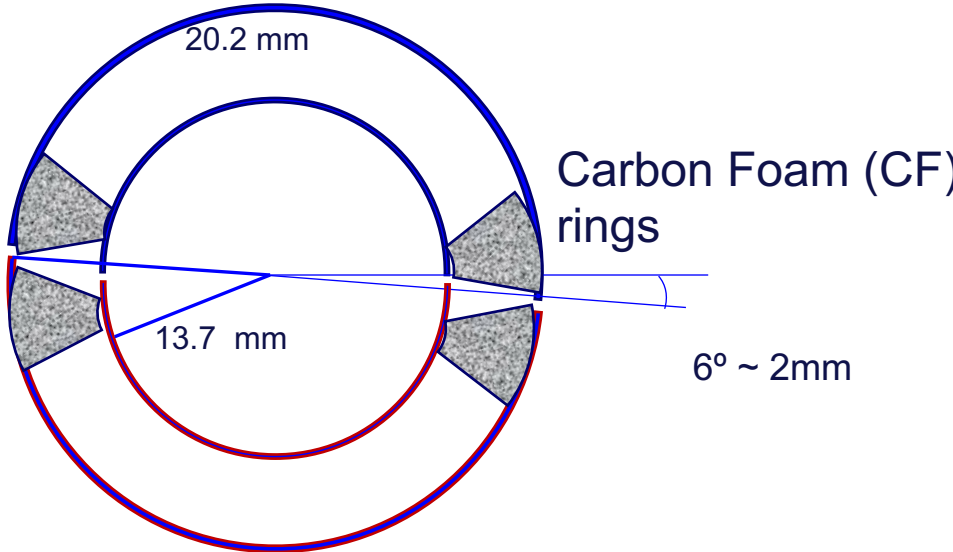
Cannot overlap sensors as in "traditional" layouts in the same layer

- Can be recovered in ϕ by rotating two layers at different radii
- Also one could twist a bit the half-layers to avoid fixed ϕ inefficiency

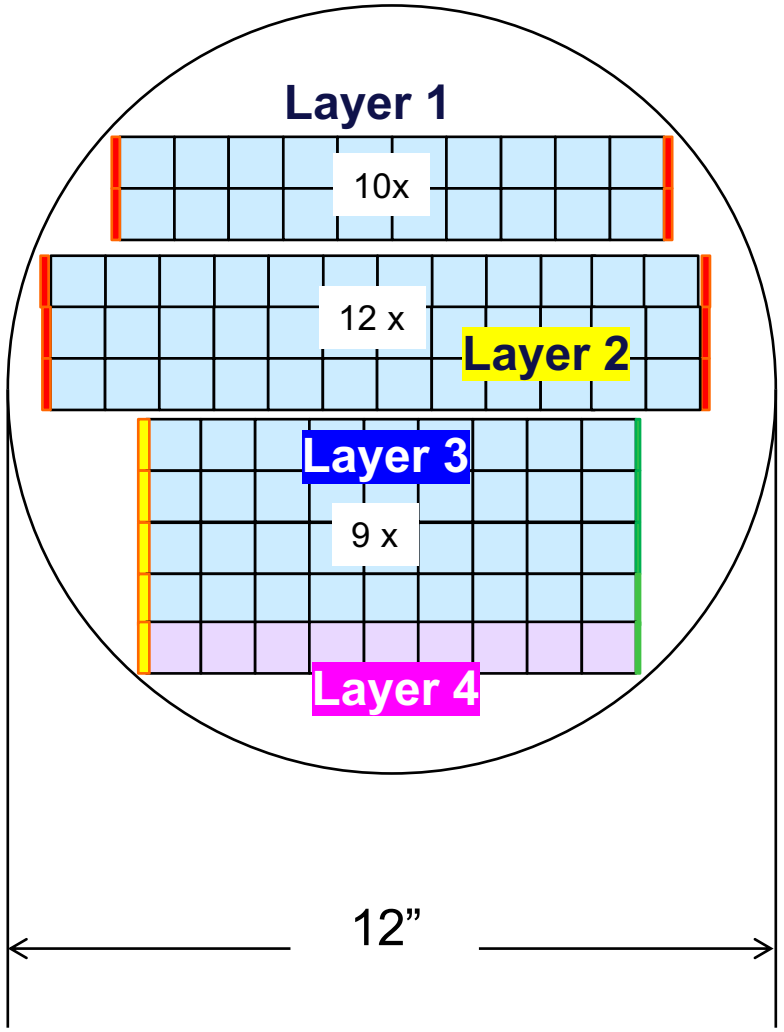
If same angular coverage for all layers is sought

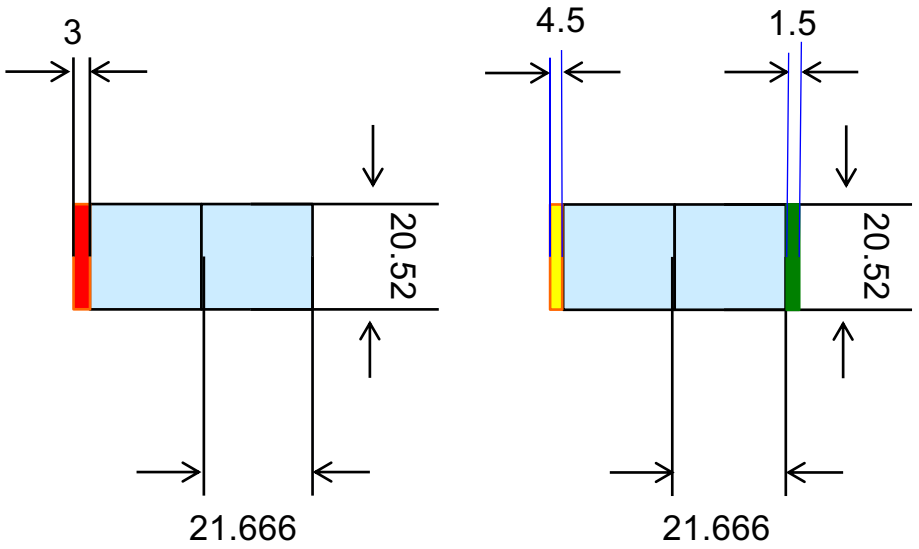
- Then needs to 2 stitched structures in z for outer layers





Same reticle for all layers





Layer 1&2 **Layer 3&4**

Layer	Radius (mm)
1	13.7
2	20.23
3	26.76
4	33.3

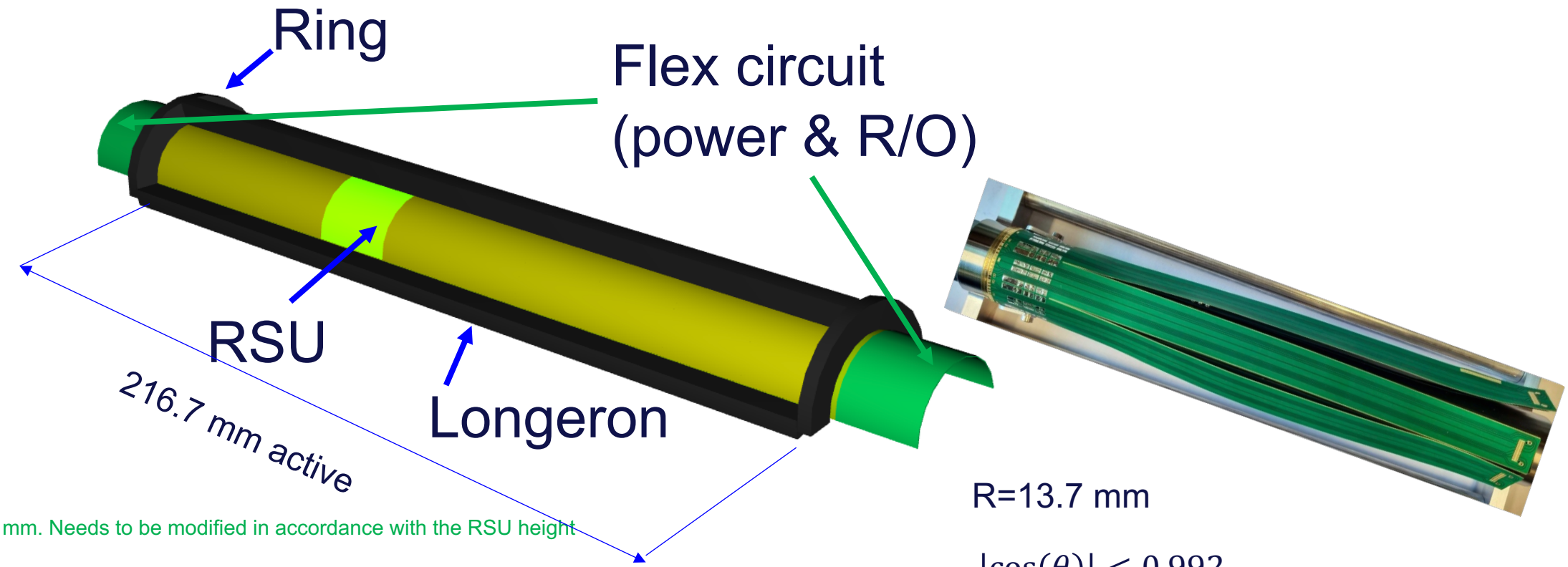
	Power density [mW cm^{-2}]		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left End Cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

Power dissipation in ITS3
(not necessarily the same for FCC-ee)

- RSU~ 50 mW/cm^2 (depends on Temp.)
- LEC ~ 700 mW/cm^2

Layer 1

- 10 RSU + 2 EC (same size) long per half layer
  - Readout and power from both sides (reduces transmission off-detector and limits power dissipation in the endcaps)
- Leaves two ~2 mm* insensitive gaps in R-phi, to account for assembly tolerances

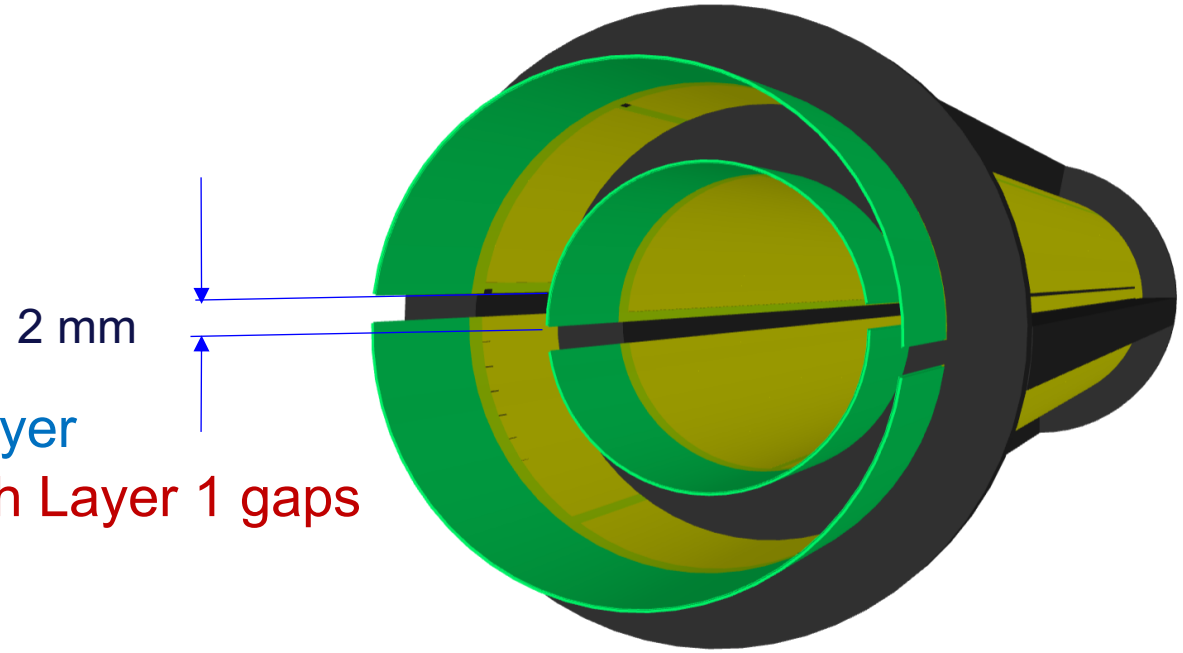


R=13.7 mm

$|\cos(\theta)| < 0.992$

* In ITS3 is 1 mm. Needs to be modified in accordance with the RSU height

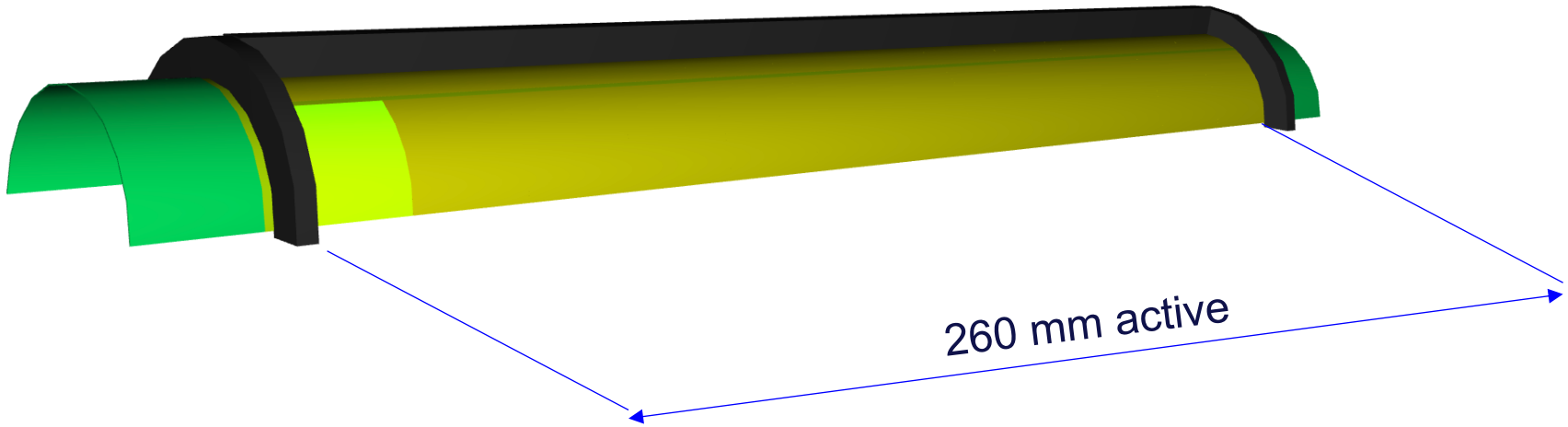
Layer 2



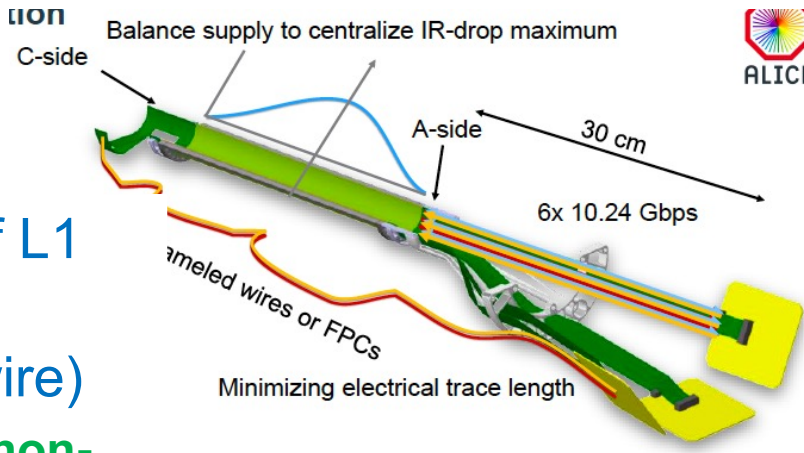
- Same as Layer 1 but 12 RSU long per half-layer
- Rotated in R-phi by ~2 mm not to overlap with Layer 1 gaps

R=20.23 mm

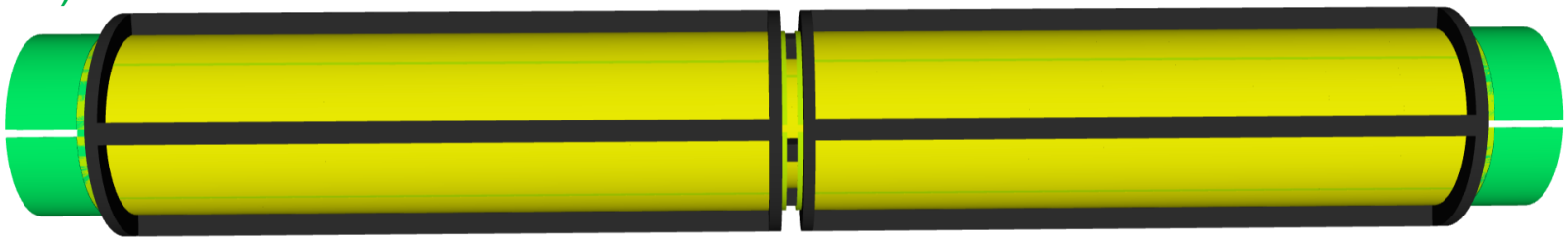
$|\cos(\theta)| < 0.988$



Layers 3 & 4



- Four "quarter" layers of 9 RSU to allow same angular coverage of L1
- Layer 4 has the same length of Layer 3 but higher radius
- Quarter readout only on one side. The other side only for power (wire)
  - Gap of ~ 2xO(10 mm) at z=0: can be mitigated by having **quarters with non-symmetric layout** (e.g. left quarter with 10 RSU and right one with 8 RSU, and swapped for L4) **or with (slightly) twisted wrap** (complicated wire bonding of the flex circuit)



Layer 3

R=26.76 mm

$|\cos(\theta)| < 0.992$

195 mm active

2x few mm

Layer 4

R=33.3 mm

$|\cos(\theta)| < 0.987$

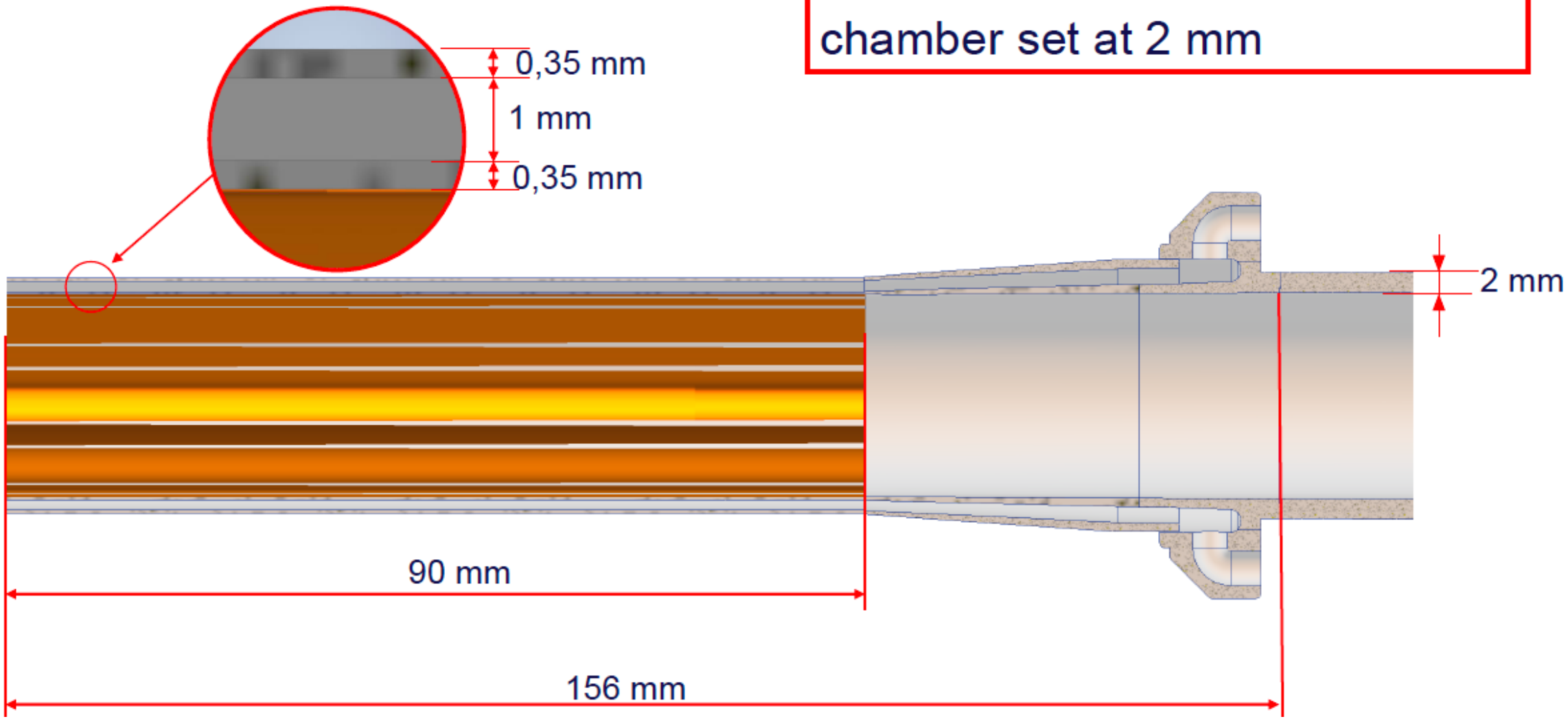
Conclusions

- **A Vertex Detector layout for IDEA (and ALLEGRO) has been engineered**
  - Uses low power, thin (50 μm) DMAPS technology
  - Integration with the machine detector elements developed
  - Services integration and cooling being finalised
  - Material budget kept at the level of $0.25\ \%\ X/X_0$ per layer
- **A much lighter concept with curved and stitched MAPS is proposed**
  - Some loss in efficiency due to stitching and folding. Impact on physics TBD
  - Optimisation of the layout ongoing following discussions with ITS3 experts
  - Cooling (air) and flex circuits routing will be addressed
  - Simulation studies on performance will be ready for the FCC-Week
    - Multiple scattering term on impact parameter decrease by a factor of ~2

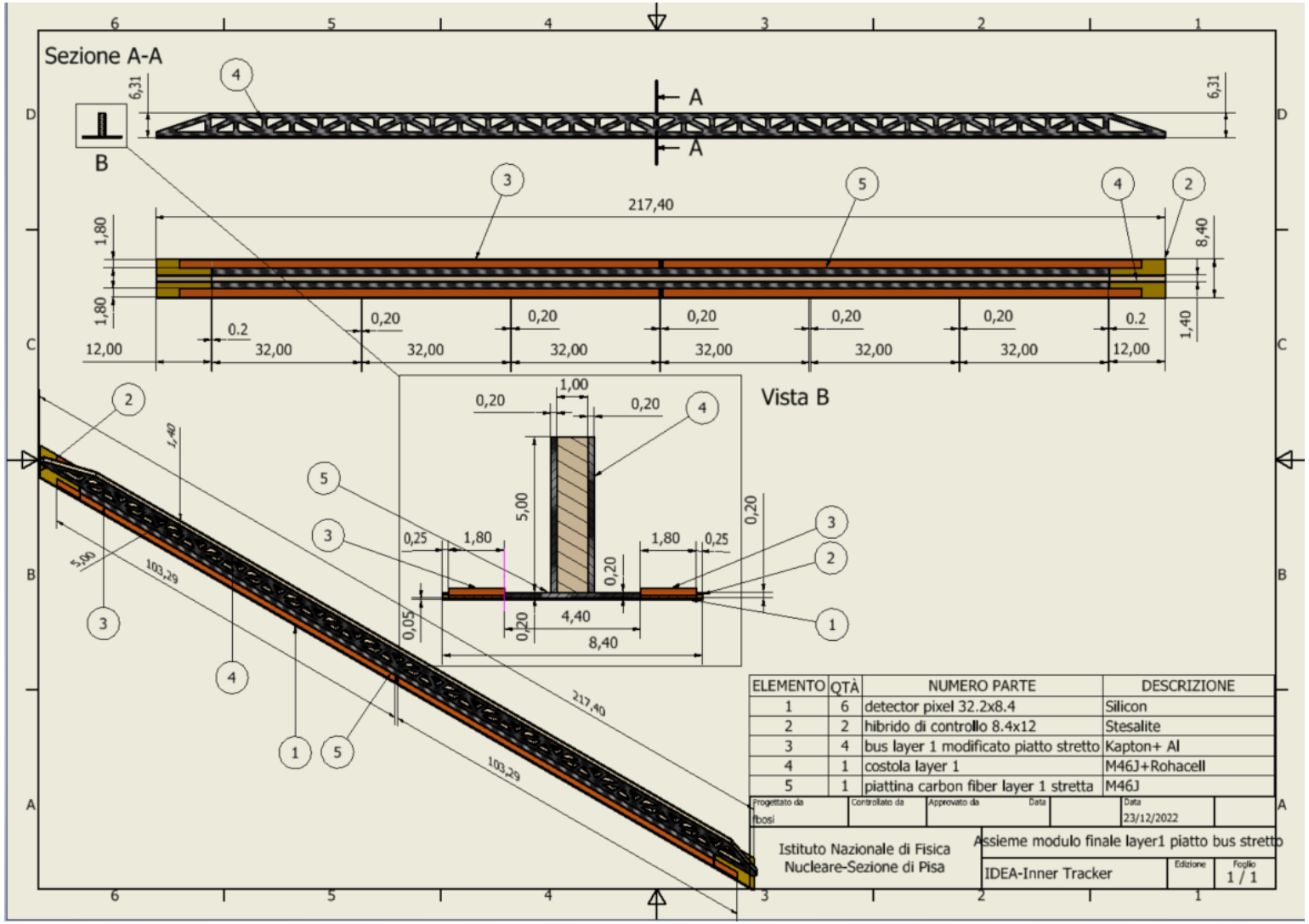
Thank you for your attention.

Thickness of the chamber

Uniform thickness of the conical chamber set at 2 mm



Layer 1 stave detail



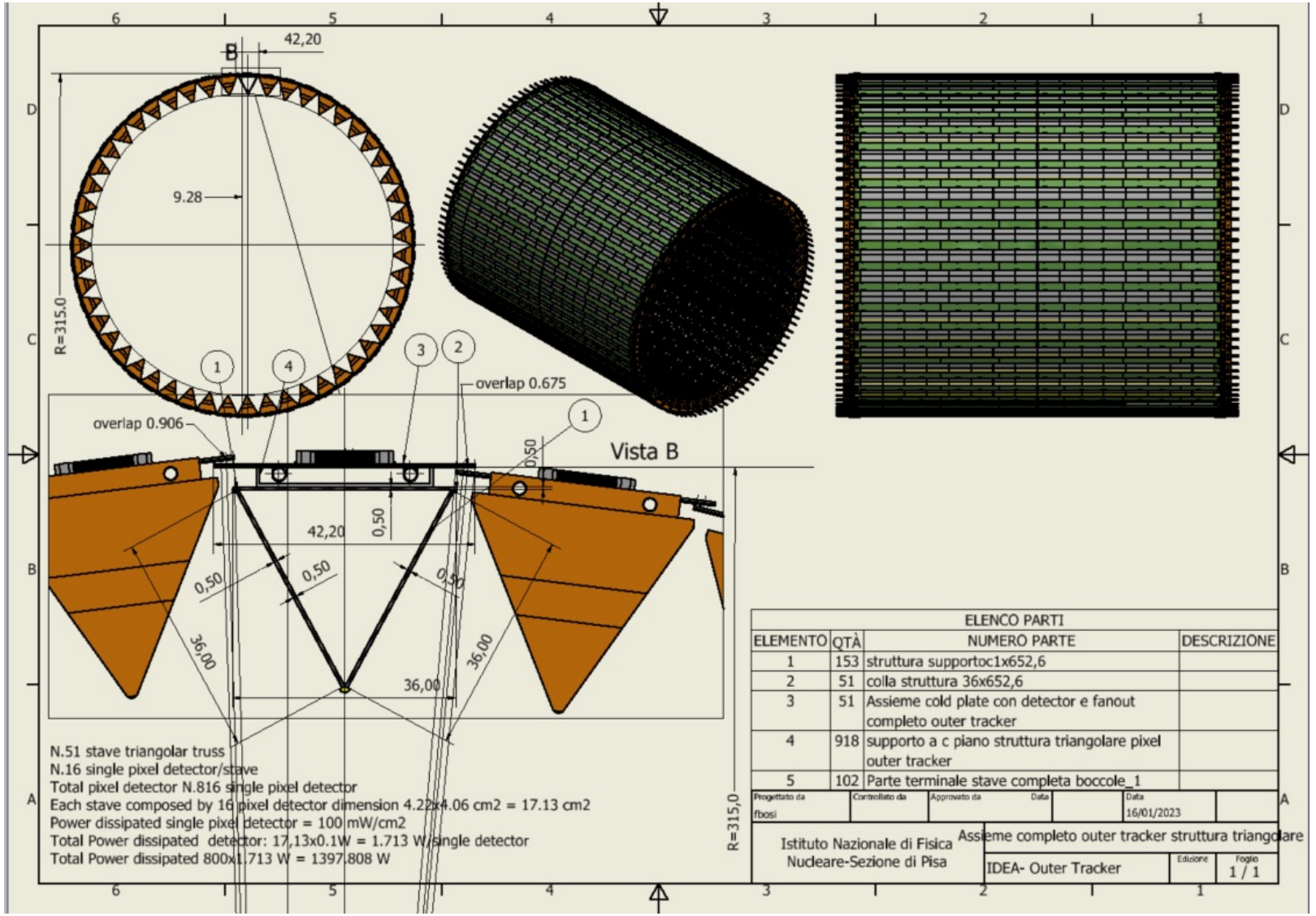
Reticular lightweight support to provide stiffness

- Thin carbon fiber walls interleaved with Rohacell
- 2 buses (data and power) 1.8 mm wide and 250 μm thick (50 μm Al, 200 μm kapton) per side
  - Inspired to low mass hybrid R&D

Sensors facing interaction point w/o any other material in front

Readout chips either sides

Air cooled



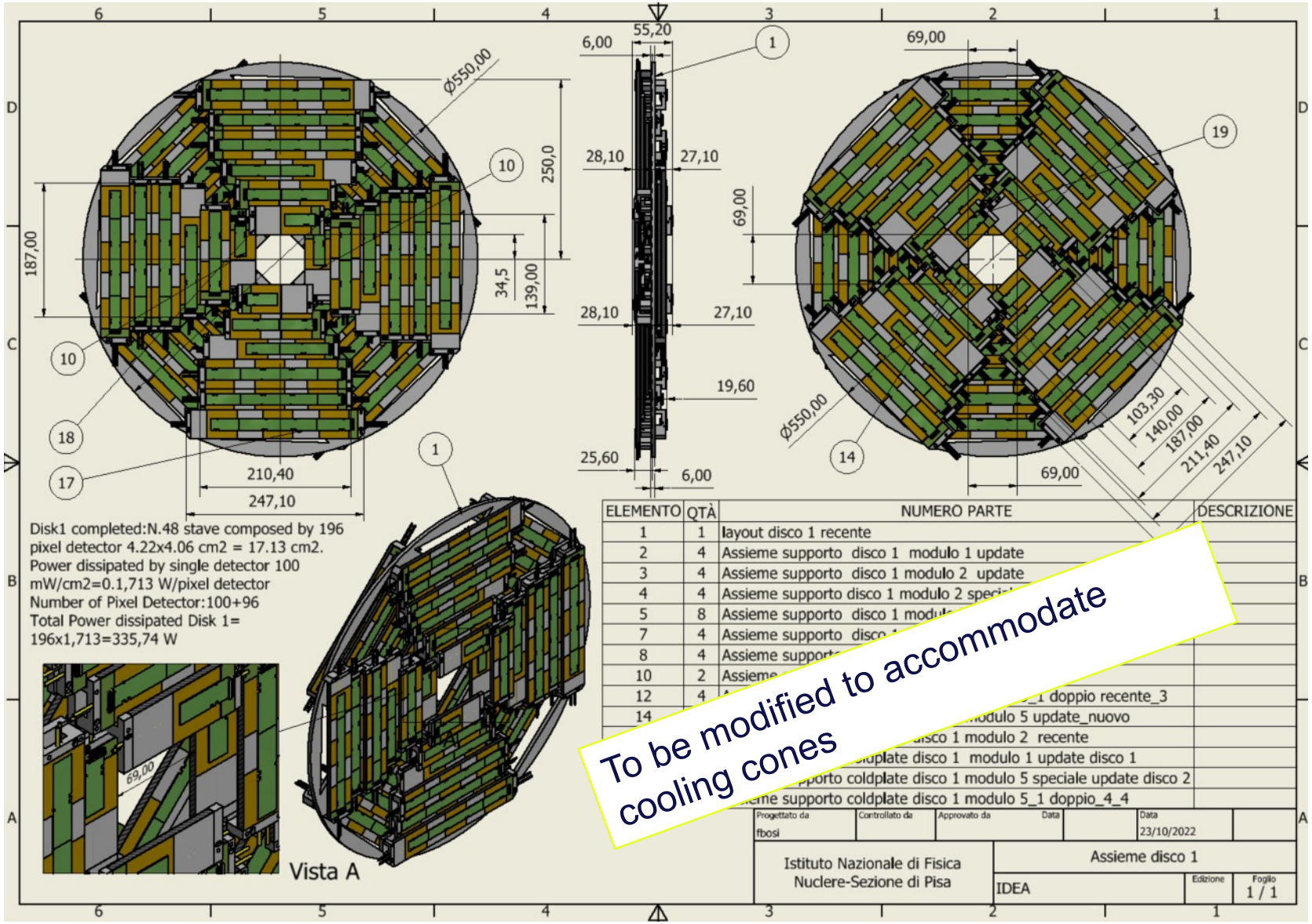
Outer Vertex Tracker Barrel
At 31.5 cm radius

51 staves of 16 modules each

Lightweight reticular support structure (ALICE/Belle-II like)

Total weight ~3.7 kg
Readout chips either side
Power budget
~1400 W

Water cooled (2 pipes of 2 mm diameter)



Outer Vertex Tracker Disk 1

2 sides (front and back) each with 4 petals.

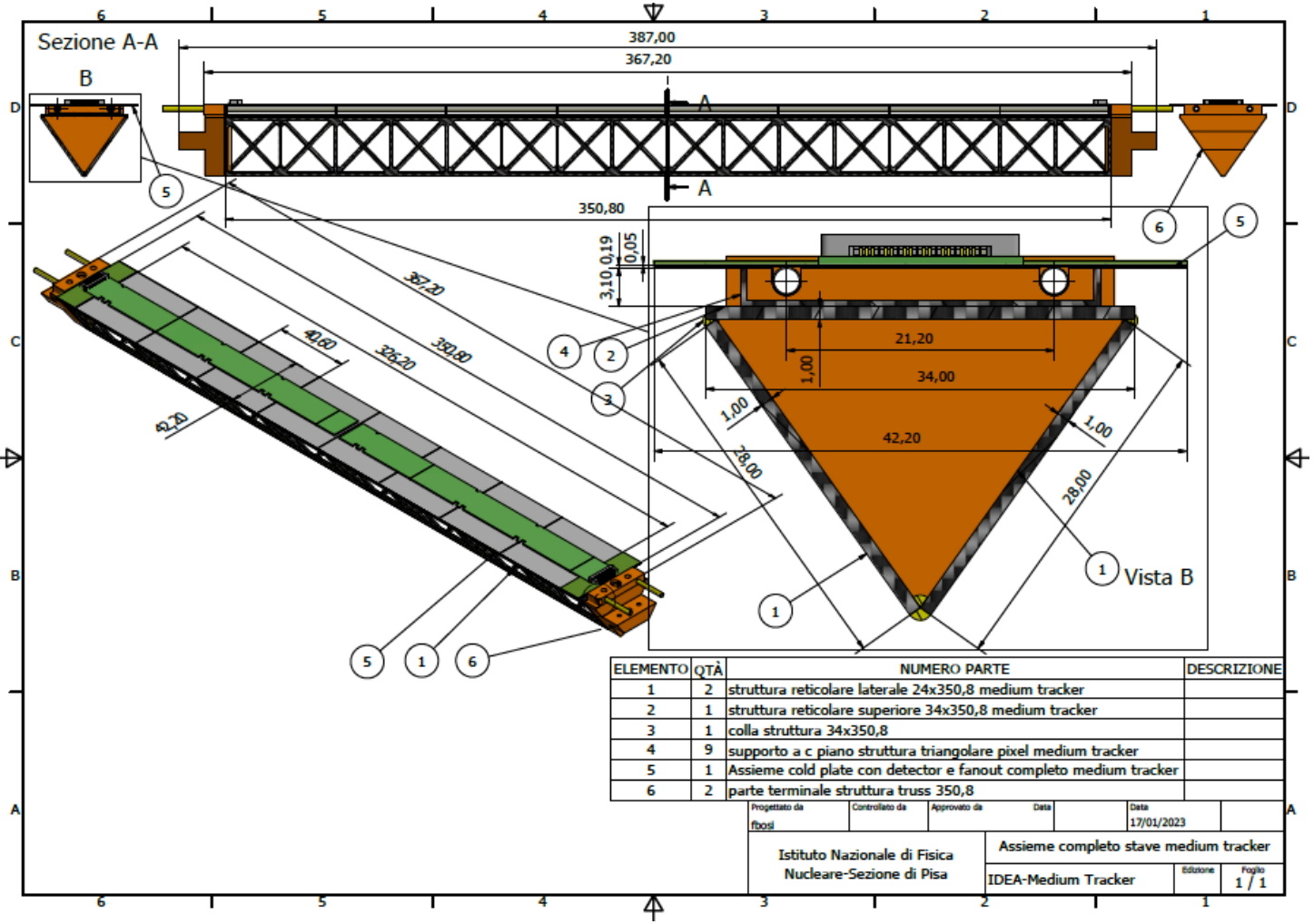
One petal is made of different staves of overlapping modules

Total modules per disk: 196
Total weight ~850 grams
Power budget ~ 336 W

Cooling using 1 water pipe (2 mm diameter)

Similar geometry for the other two disks

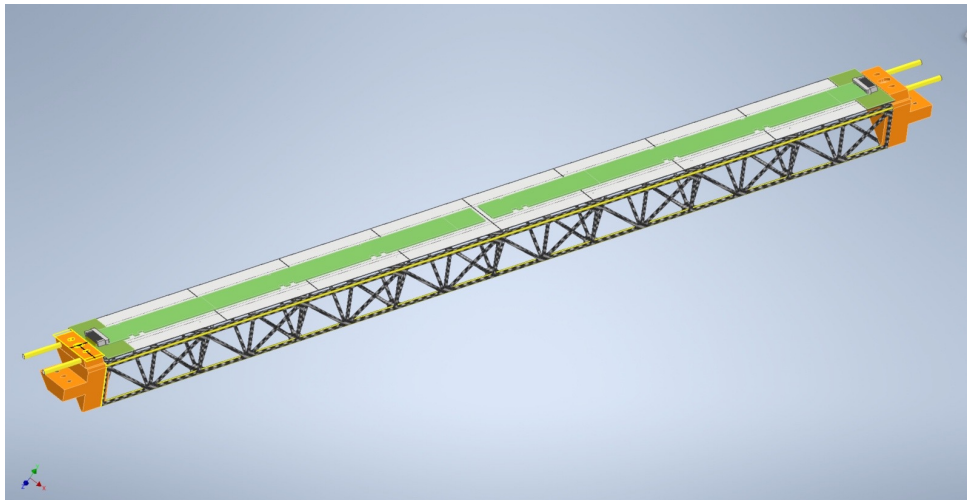
Stave detail

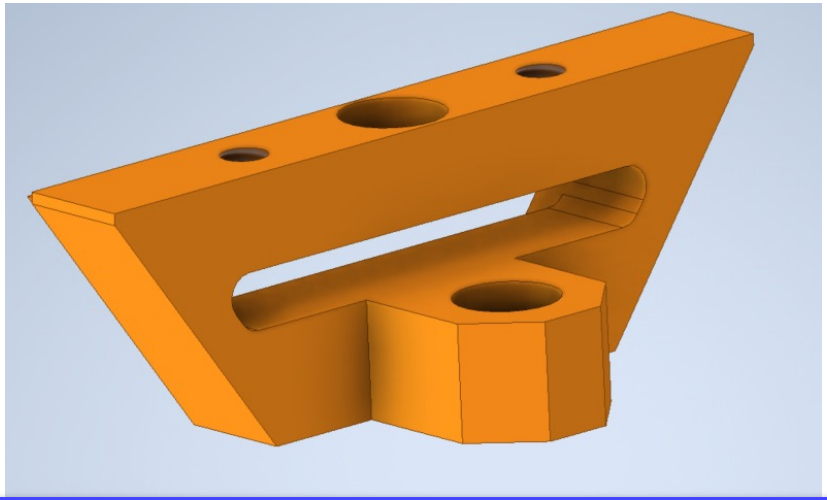


ELEMENTO	QTÀ	NUMERO PARTE	DESCRIZIONE
1	2	struttura reticolare laterale 24x350,8 medium tracker	
2	1	struttura reticolare superiore 34x350,8 medium tracker	
3	1	colla struttura 34x350,8	
4	9	supporto a c piano struttura triangolare pixel medium tracker	
5	1	Assieme cold plate con detector e fanout completo medium tracker	
6	2	parte terminale struttura truss 350,8	

Progettato da	Controllato da	Approvato da	Data	Data
fbosi				17/01/2023

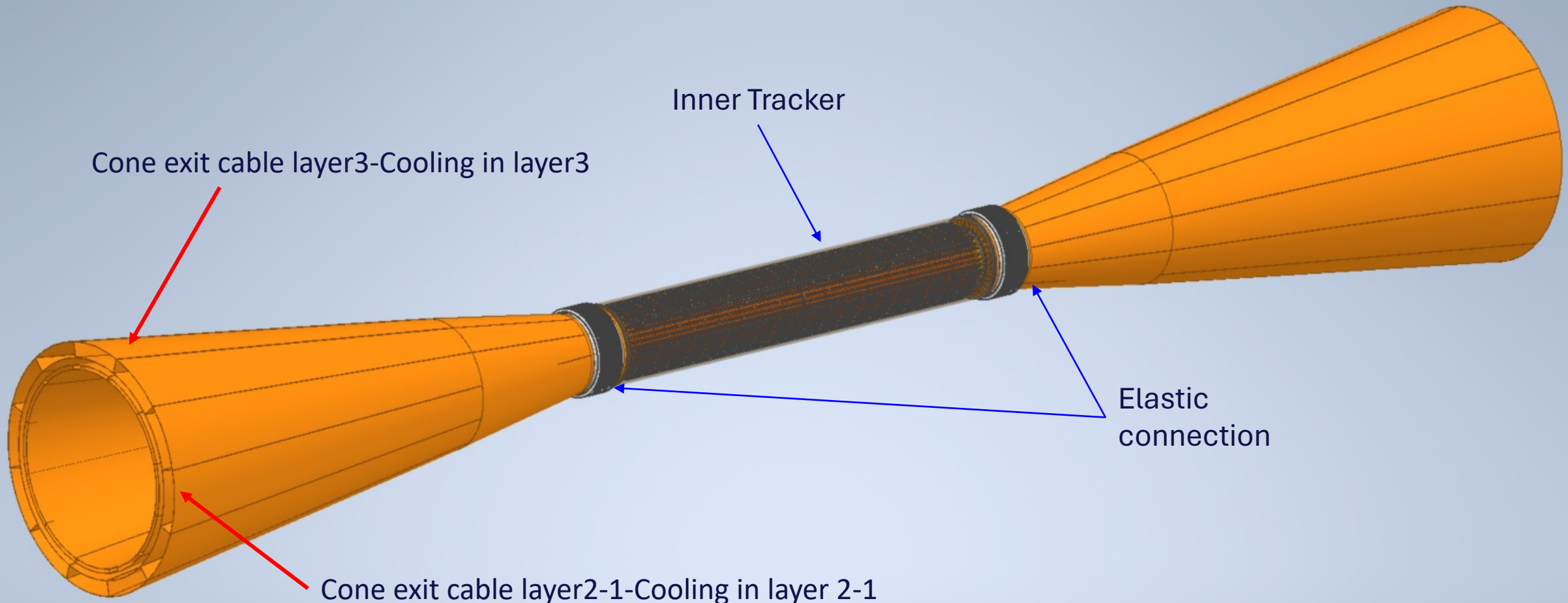
Istituto Nazionale di Fisica Nucleare-Sezione di Pisa	Assieme completo stave medium tracker	
	IDEA-Medium Tracker	Edizione / Foglio 1 / 1

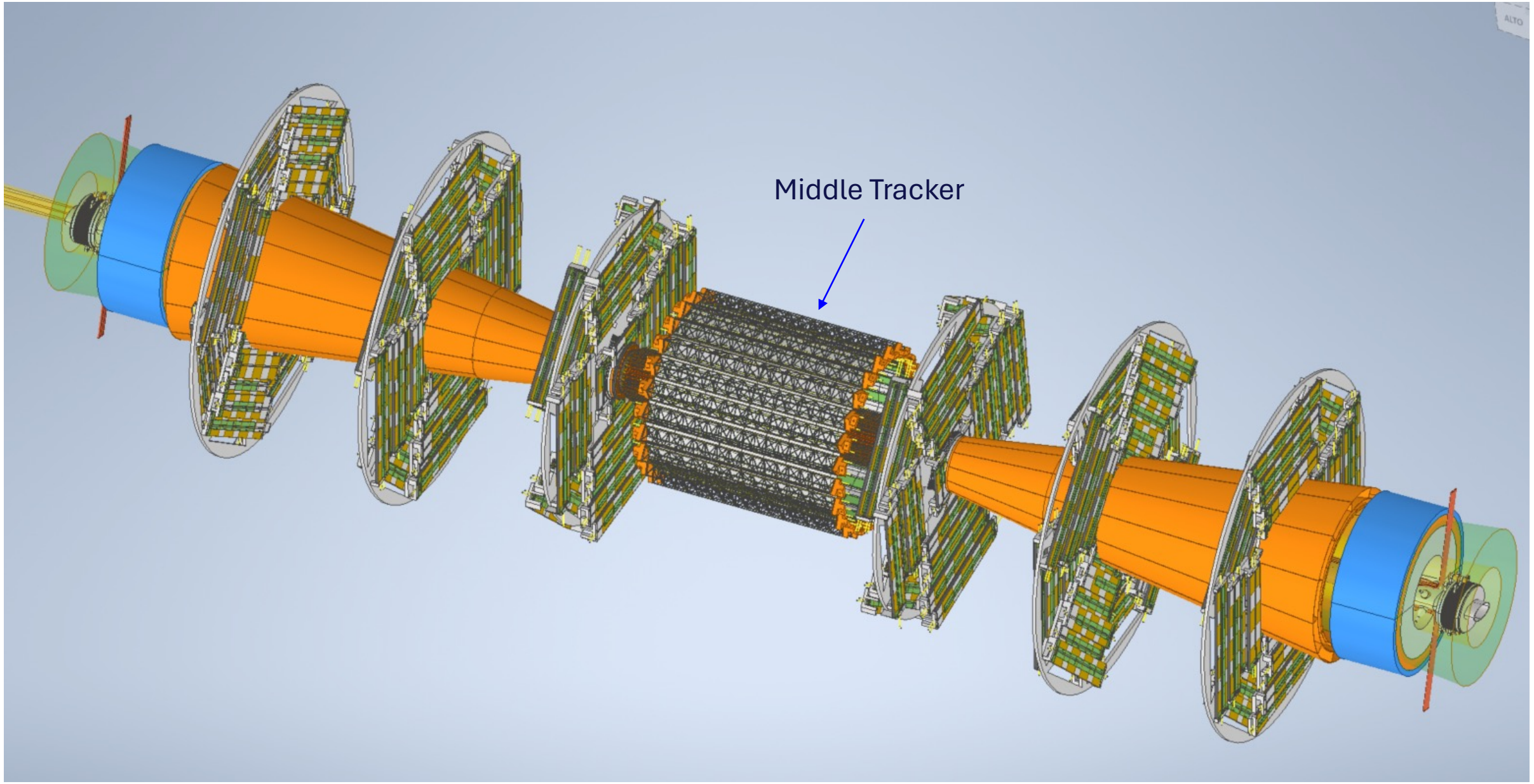


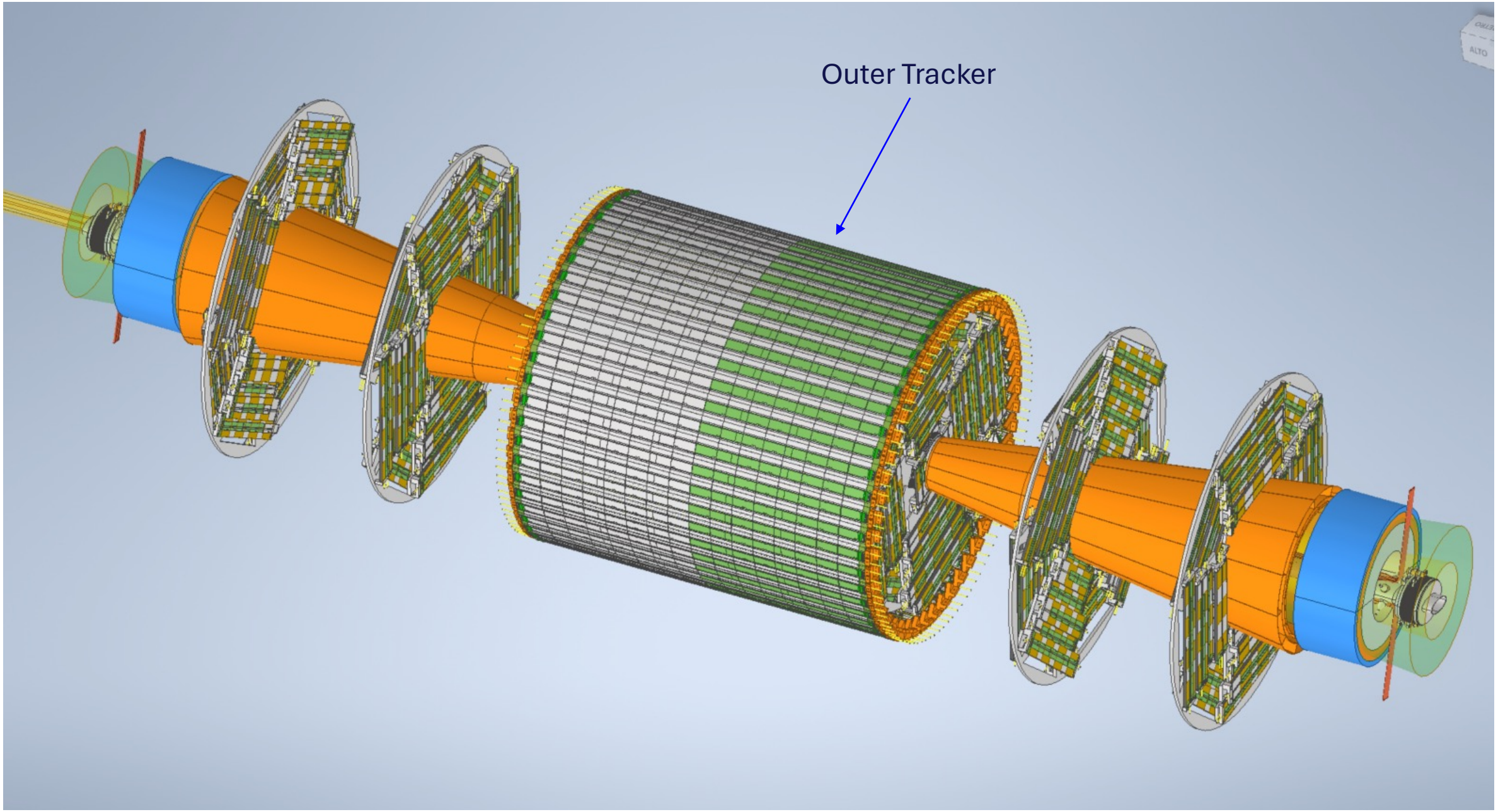


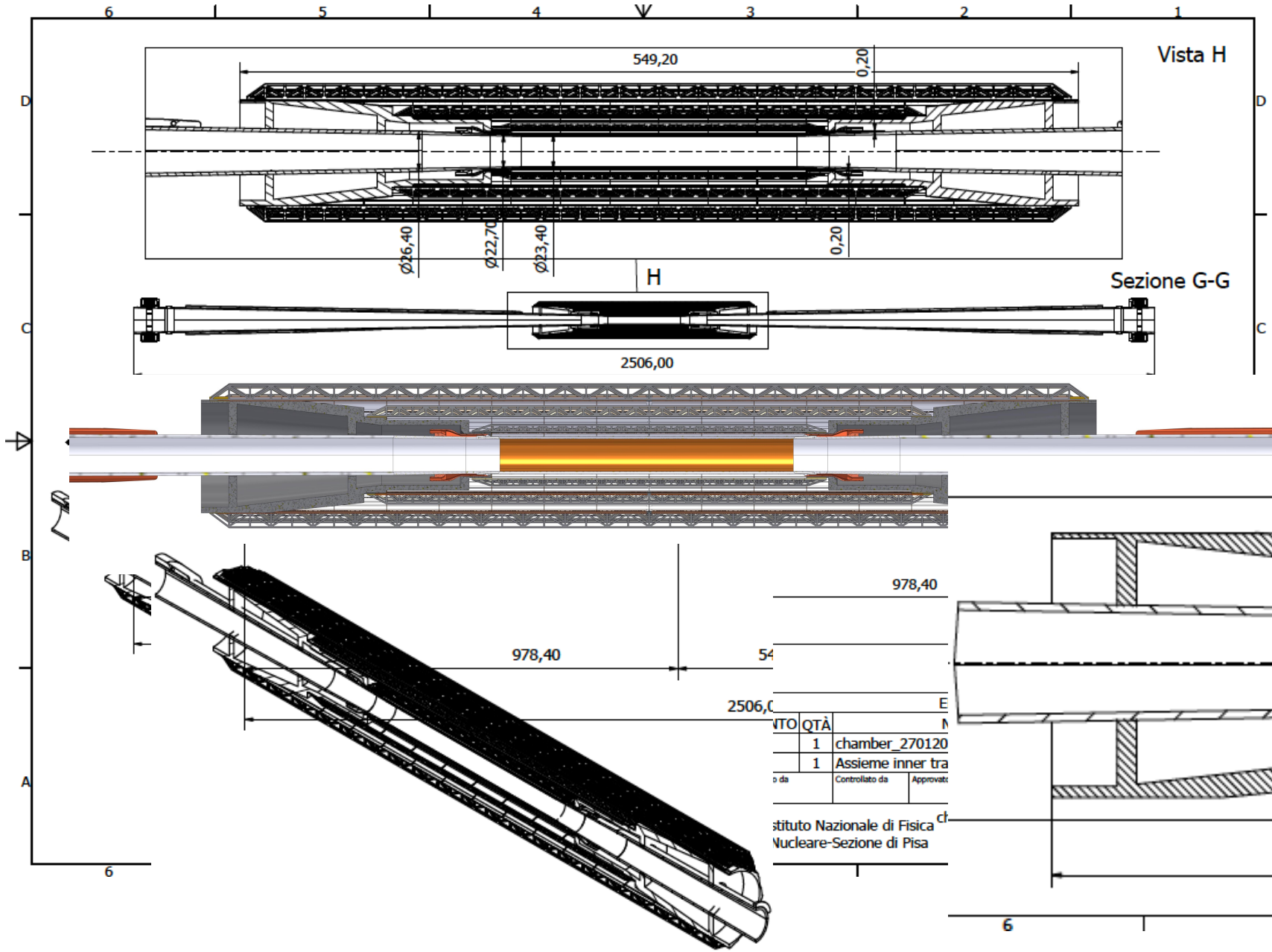
Shaped to minimize material at the end of the stave

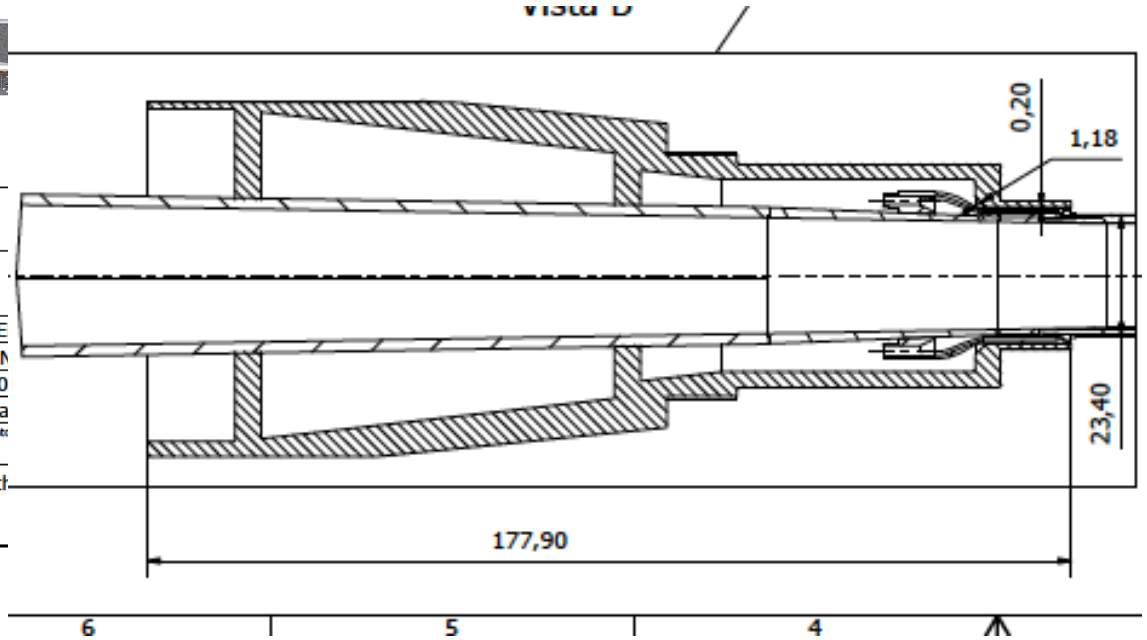
Service cones for cooling and cables




Middle Tracker


Outer Tracker





Inner vertex detector supporting conical structures on elliptical chamber
~450 grams

Engineered for air ducts and thermal isolation from the beam pipe during bakeout

View from Lumical

Cable tunnel Layer 3

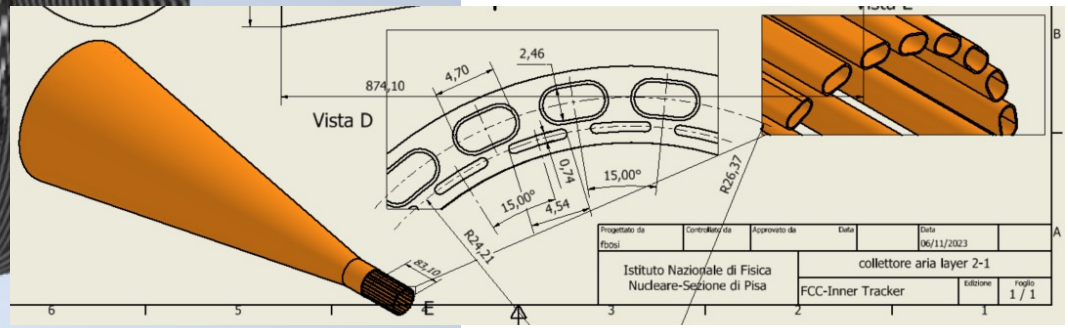
Air cooling Layer 3

Cable tunnel Layer 2-1

Air cooling Layer 2-1

Peek Insert 1

Peek Insert 2



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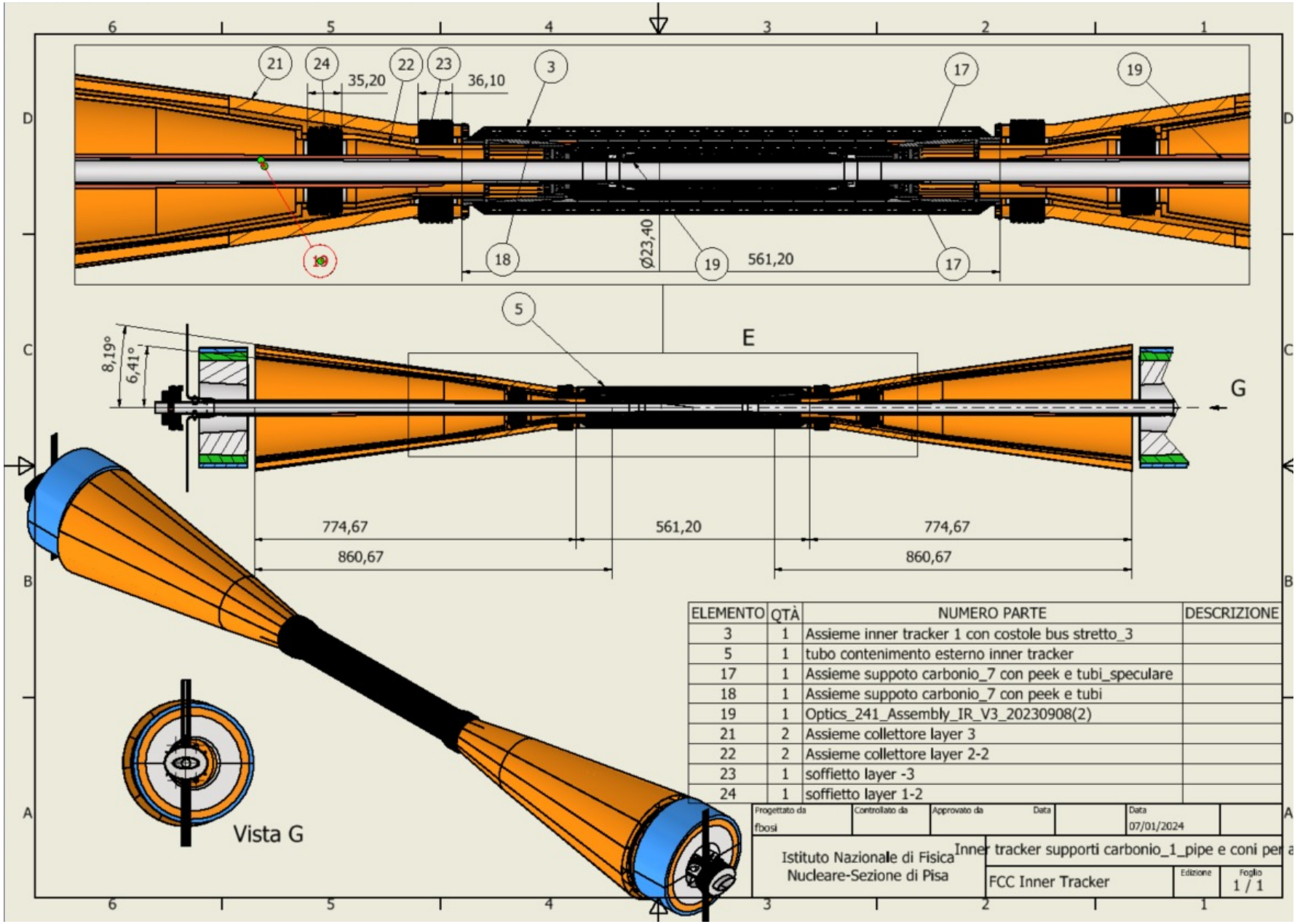

ELEMENTO	QTÀ	NUMERO PARTE	DESCRIZIONE
3	1	Assieme inner tracker 1 con costole bus stretto_3	
5	1	tubo contenimento esterno inner tracker	
17	1	Assieme suppoto carbonio_7 con peek e tubi_speculare	
18	1	Assieme suppoto carbonio_7 con peek e tubi	
19	1	Optics_241_Assembly_IR_V3_20230908(2)	
21	2	Assieme collettore layer 3	
22	2	Assieme collettore layer 2-2	
23	1	soffietto layer -3	
24	1	soffietto layer 1-2	

Progettato da	Controllato da	Approvato da	Data		Data	
fbosi					07/01/2024	

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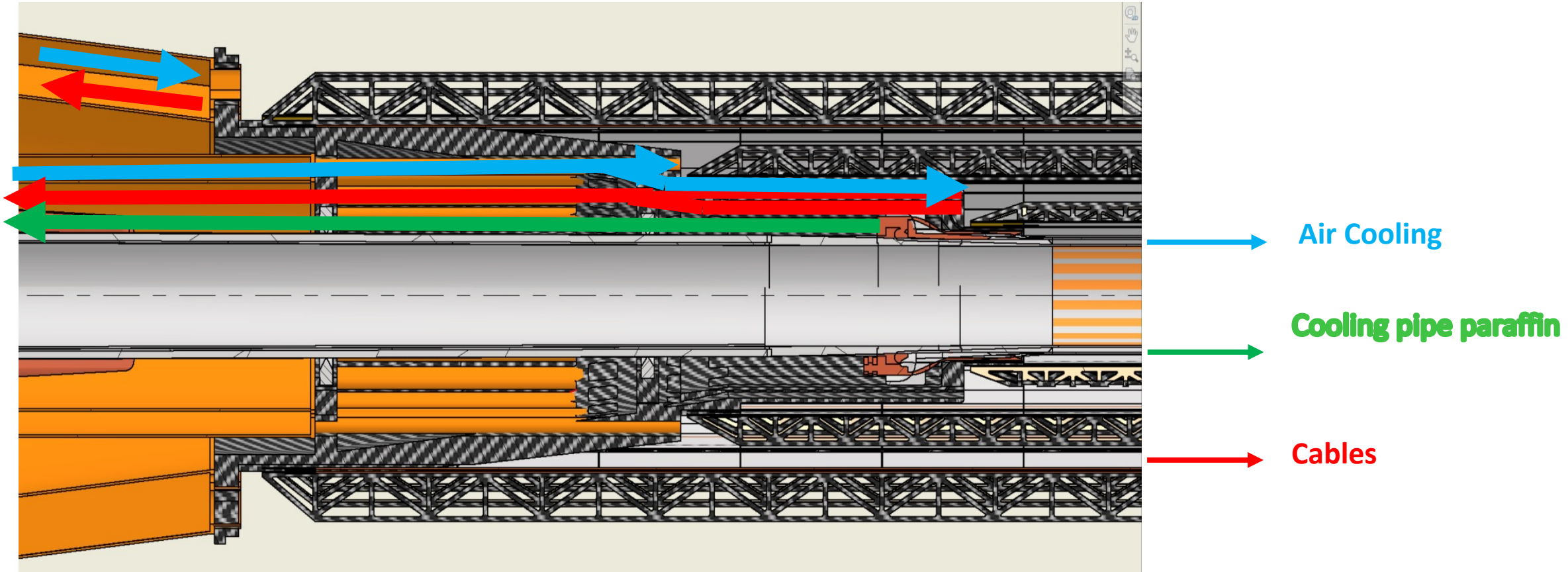
Inner tracker supporti carbonio_1_pipe e coni per a

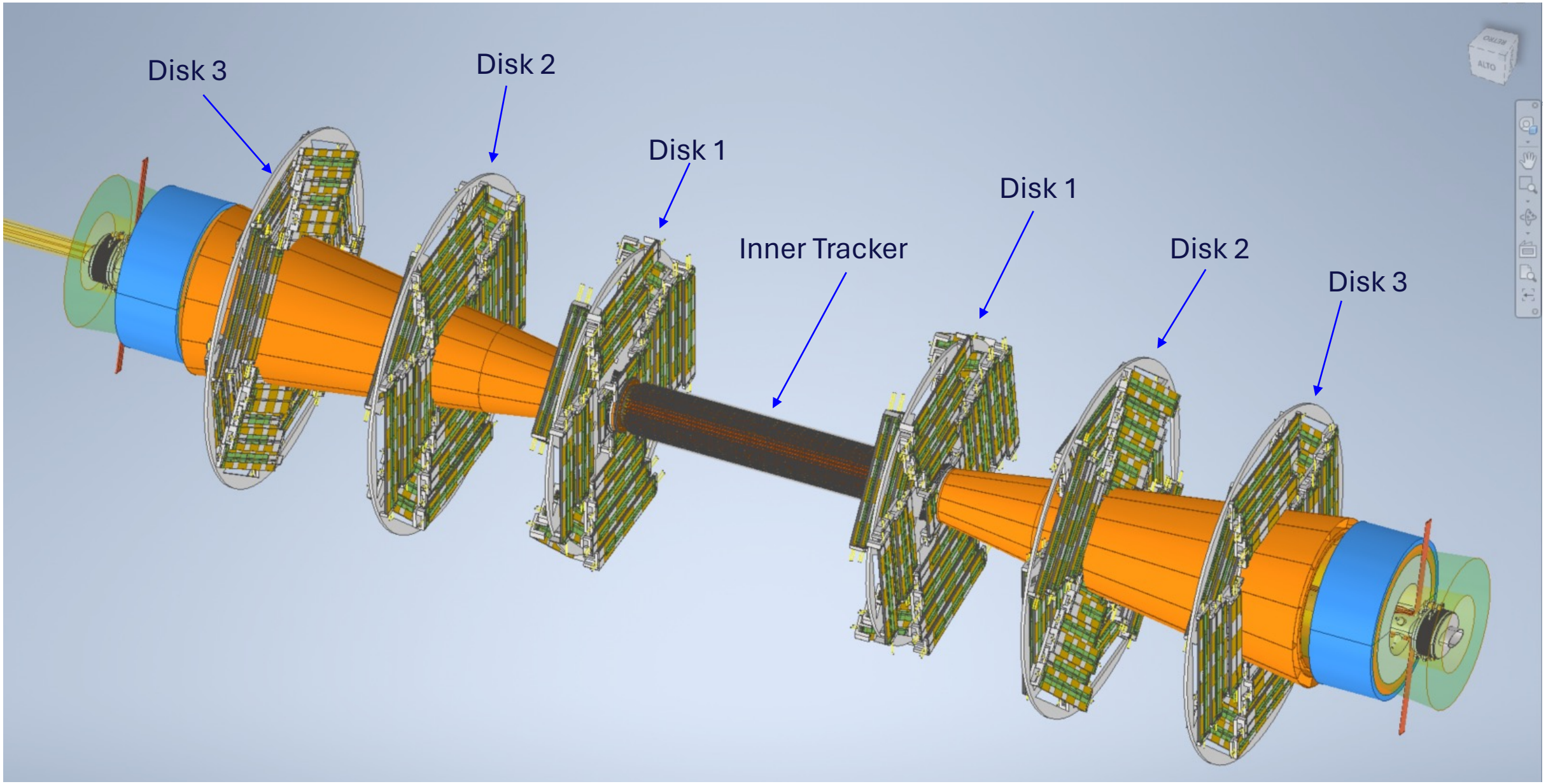
FCC Inner Tracker

Edizione

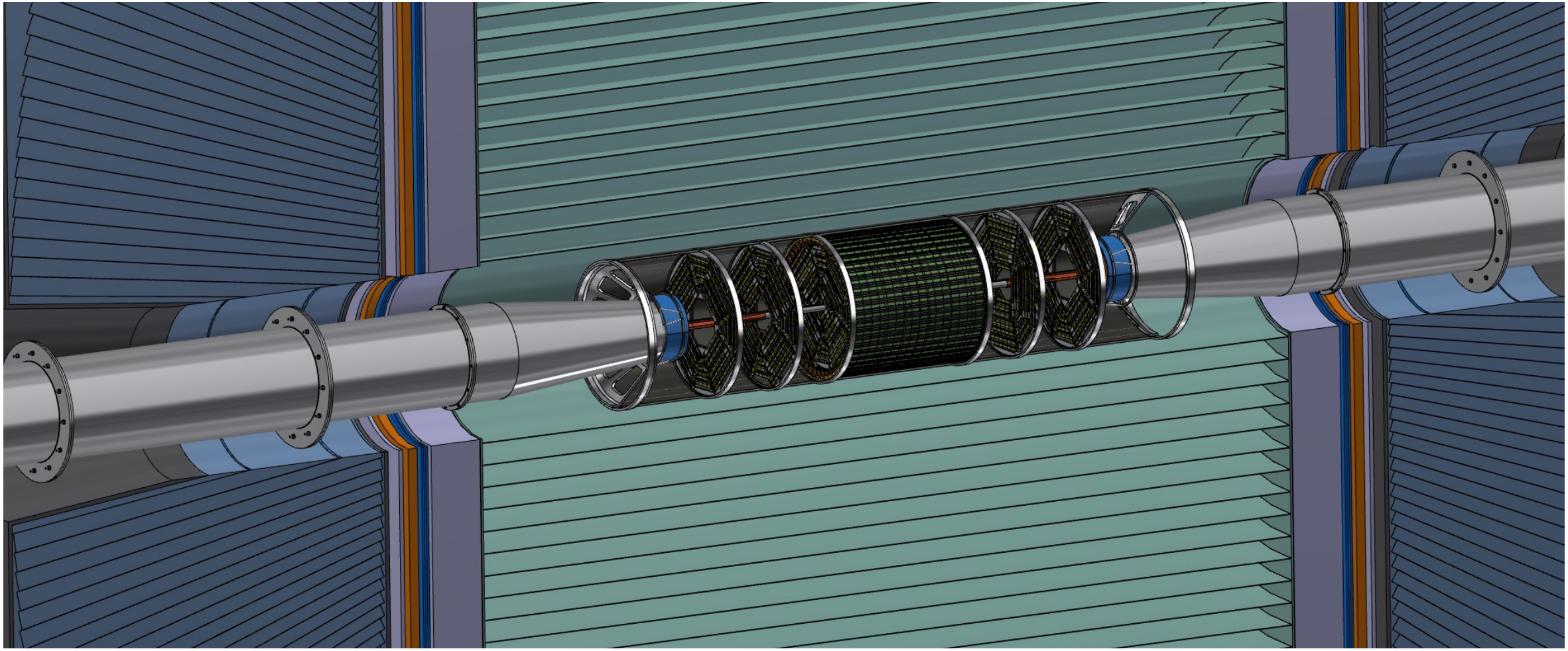
Foglio 1 / 1

Integration with beam pipe cooling manifold



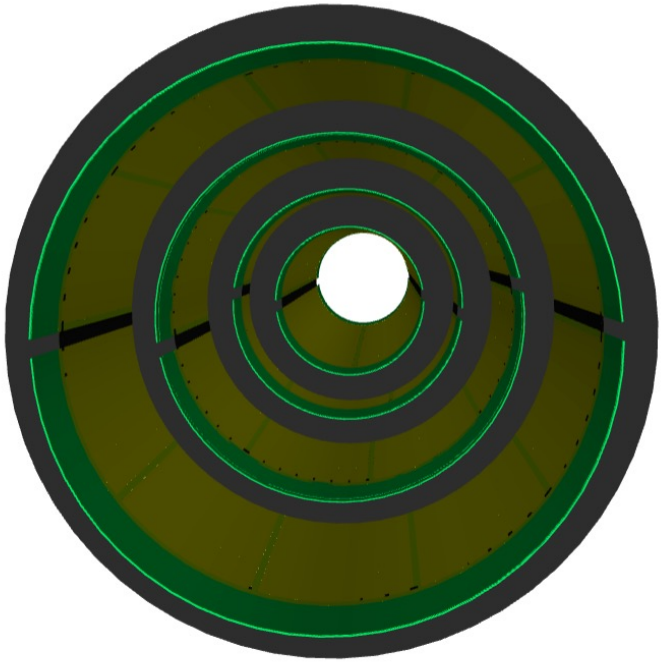

Disk 3
Disk 2
Disk 1
Inner Tracker
Disk 1
Disk 2
Disk 3

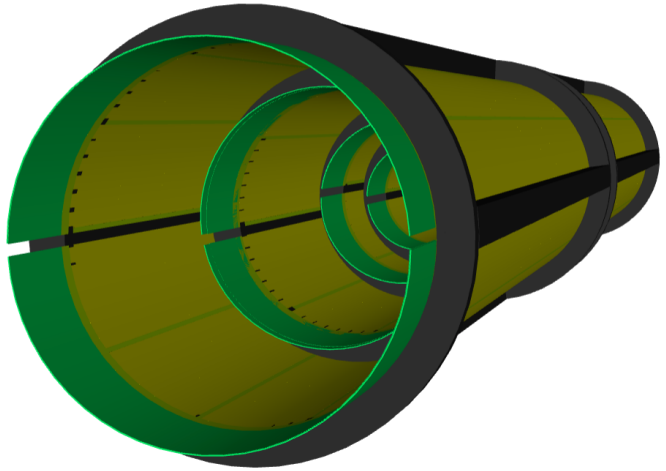
General integration

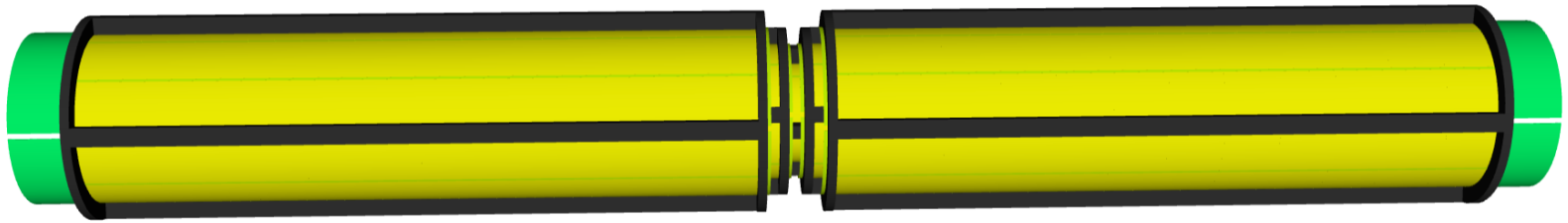


Alternative Layer 4

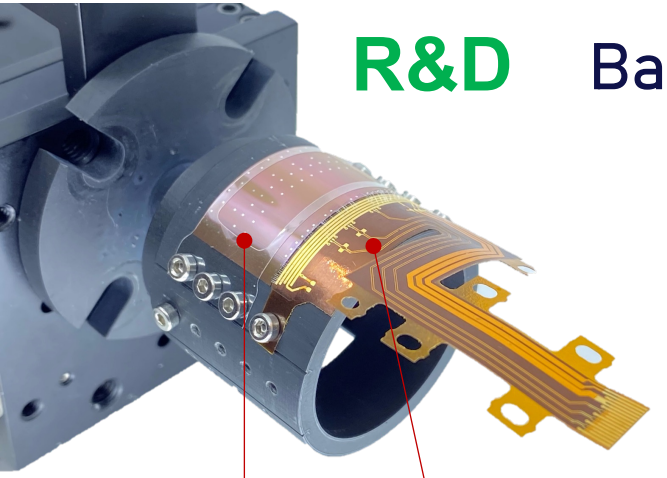
- In case the same acceptance for a 4th layer is sought, then the four “quarter” layers are made of 12 RSU.
- However, one cannot compensate the gap at z=0 with unequal left and right quarters, since 13 RSU cannot be made in 6 rows in a 12” wafer.
- One possible compensation could be to spread the gap at different z by twisting the quarters of a few mm: doable, but one complicates the bonding of the flex circuits



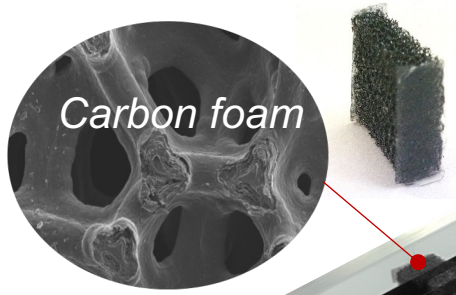




R&D Based on present effort in the design of the ITS3 (RUN4 –LS3)

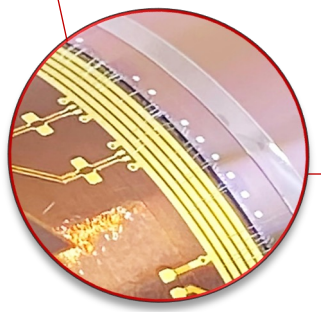


➔ minimum material support and gas cooling

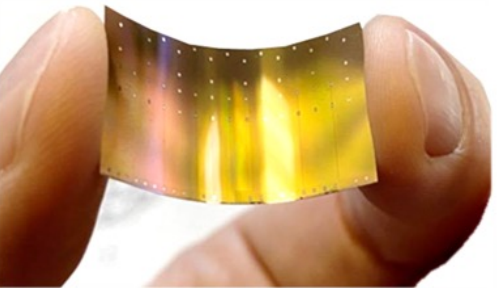


L0 L1 L2

➔ Wire bonding at the edge side



➔Curved Silicon sensors



➔ Chip stitching