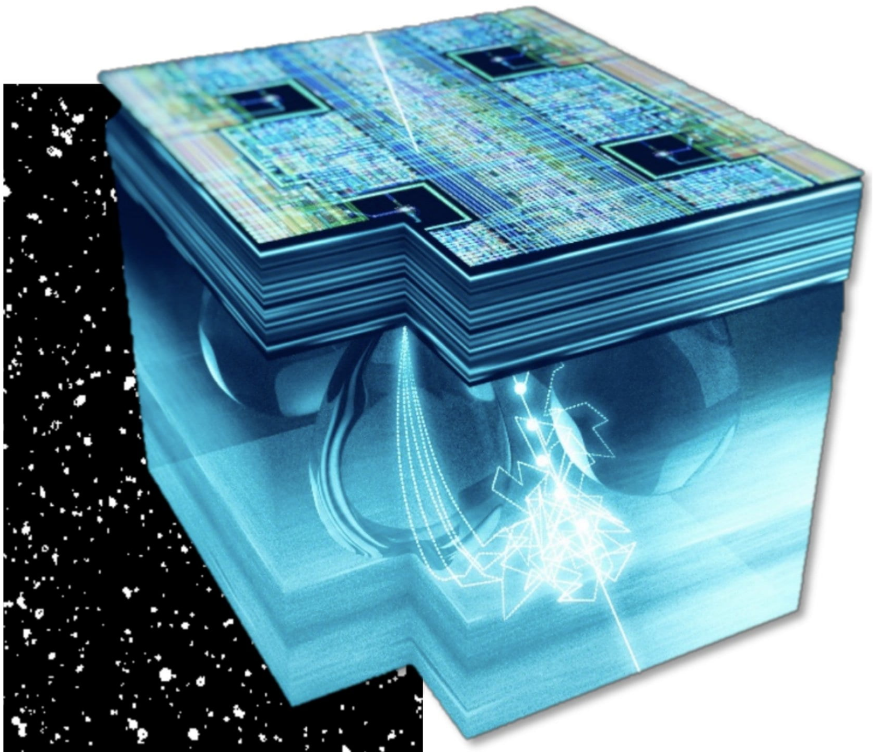
A new Pixel lab for ELementary Physics at MIT

focus on the MAPS-based SVT detector for the EIC



Gian Michele Innocenti (MIT)

US FCC Workshop 2024

MIT, March 25-27, 2024

https://pixelphilab.mit.edu

Overview of the talk

Brief introduction to MAPS technology for HEP

The Silicon Vertex Tracker for the ePIC experiment at the EIC

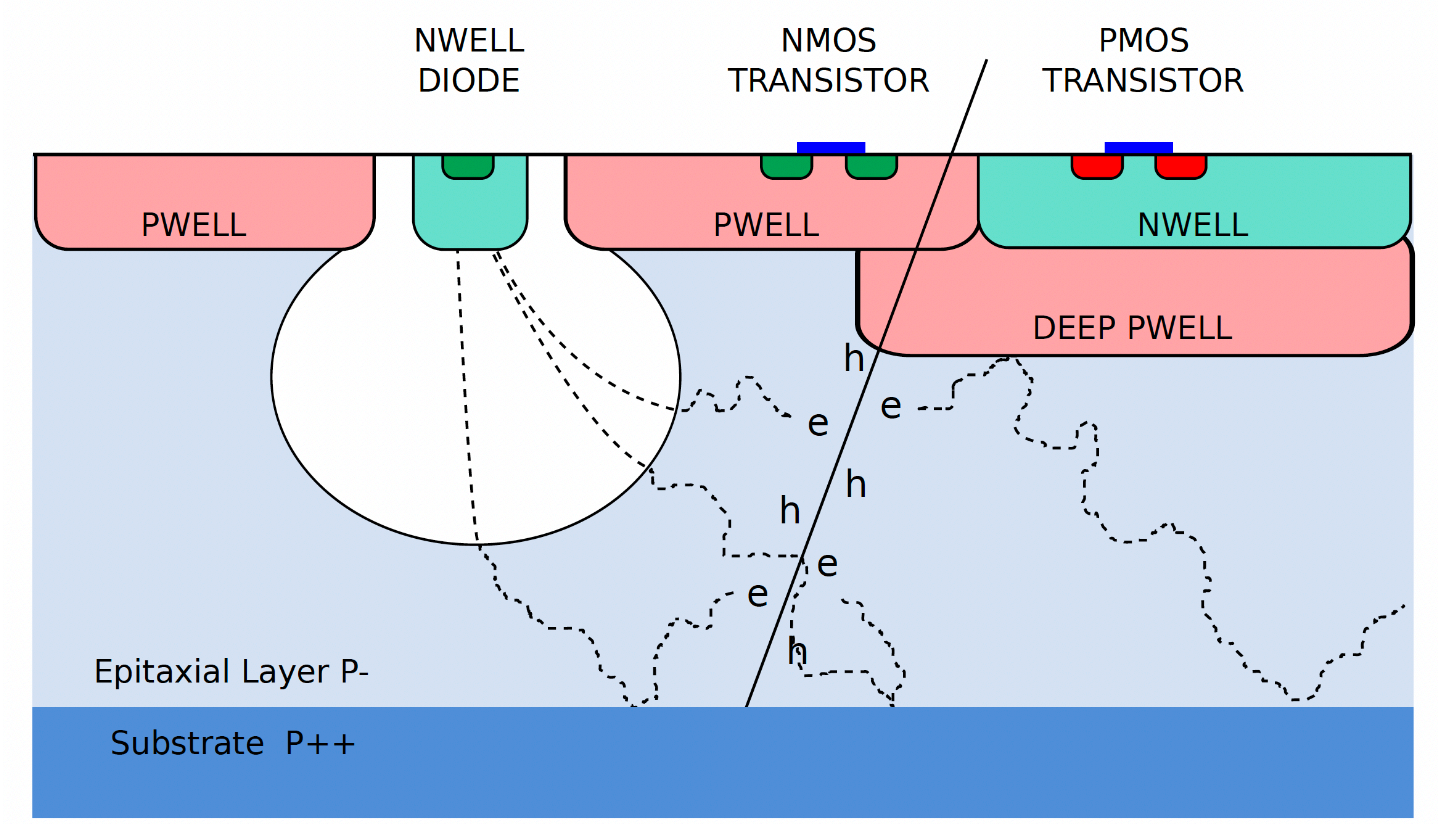
- stitched MAPS sensors for ITS3 and SVT
- detector overview
- technological challenges and ongoing R&D

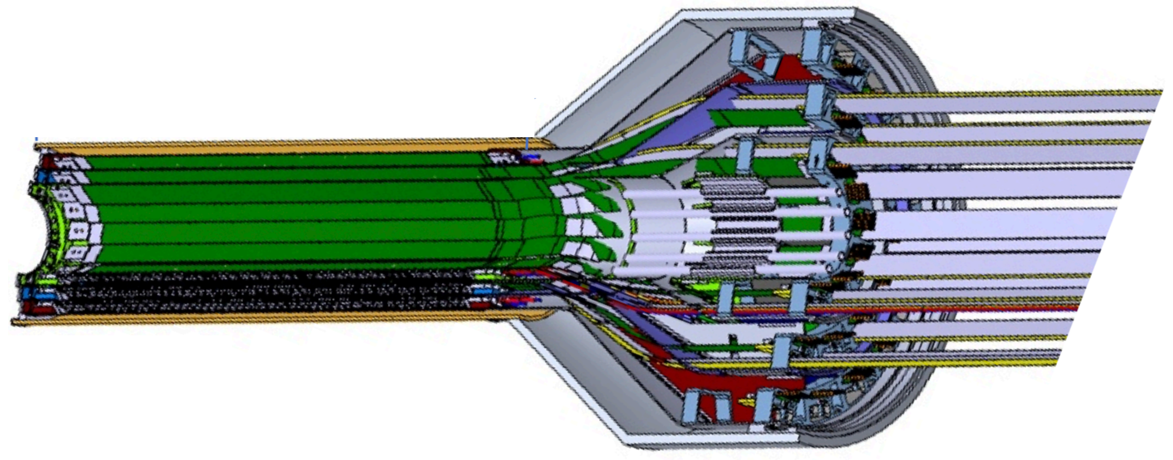
PixELphi lab at MIT for SVT and beyond

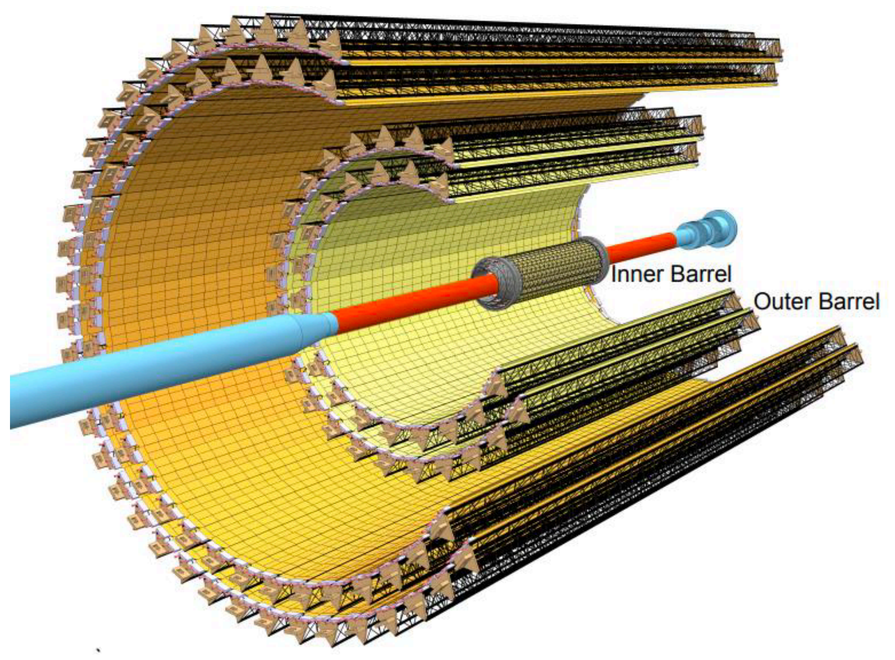
- MAPS technology for elementary particle and nuclear physics

MAPS technology for ALICE ITS2 and sPHENIX MVTX

ITS3, J. Phys. G: Nucl. Part. Phys. 41 087002 (2014)

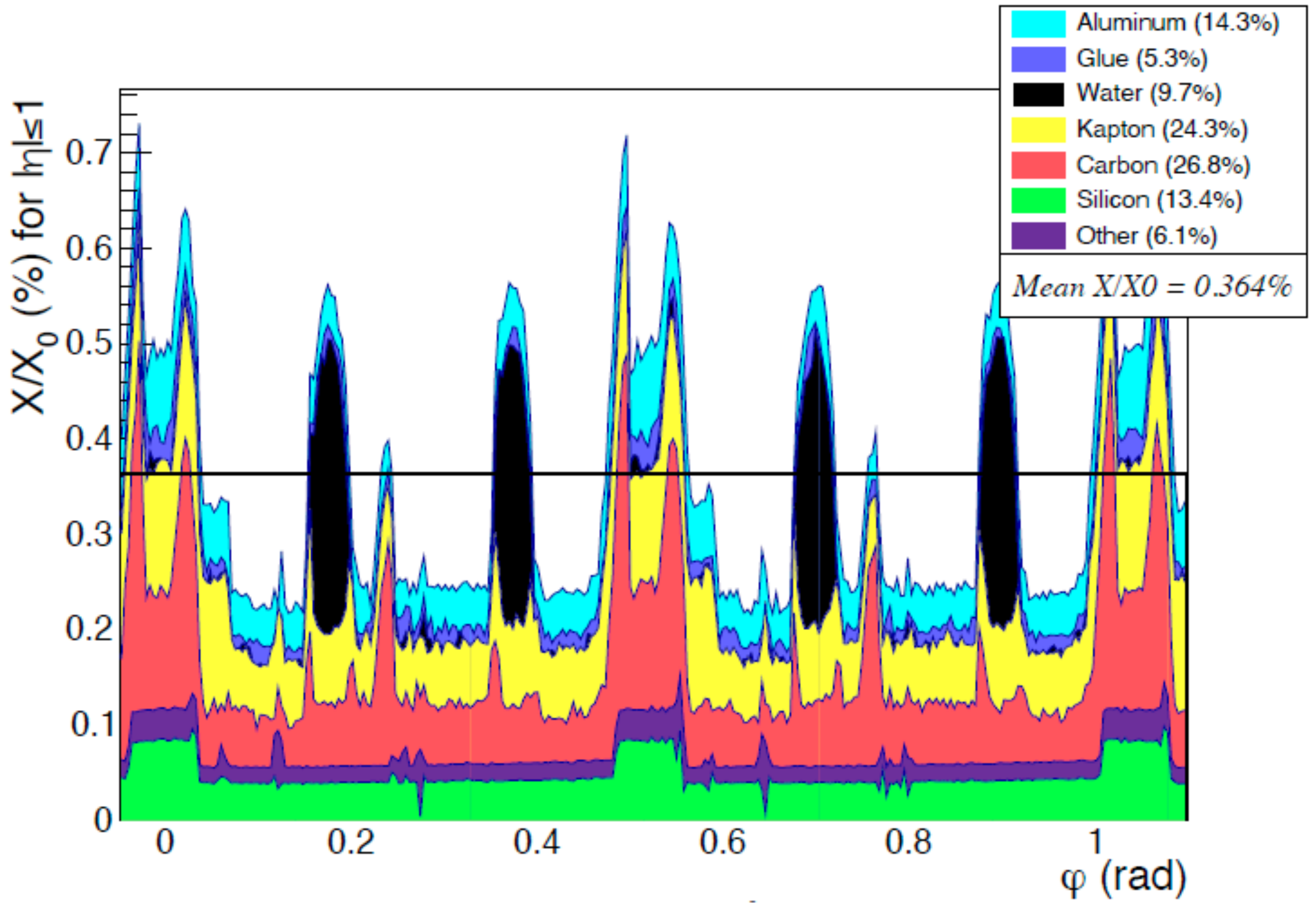


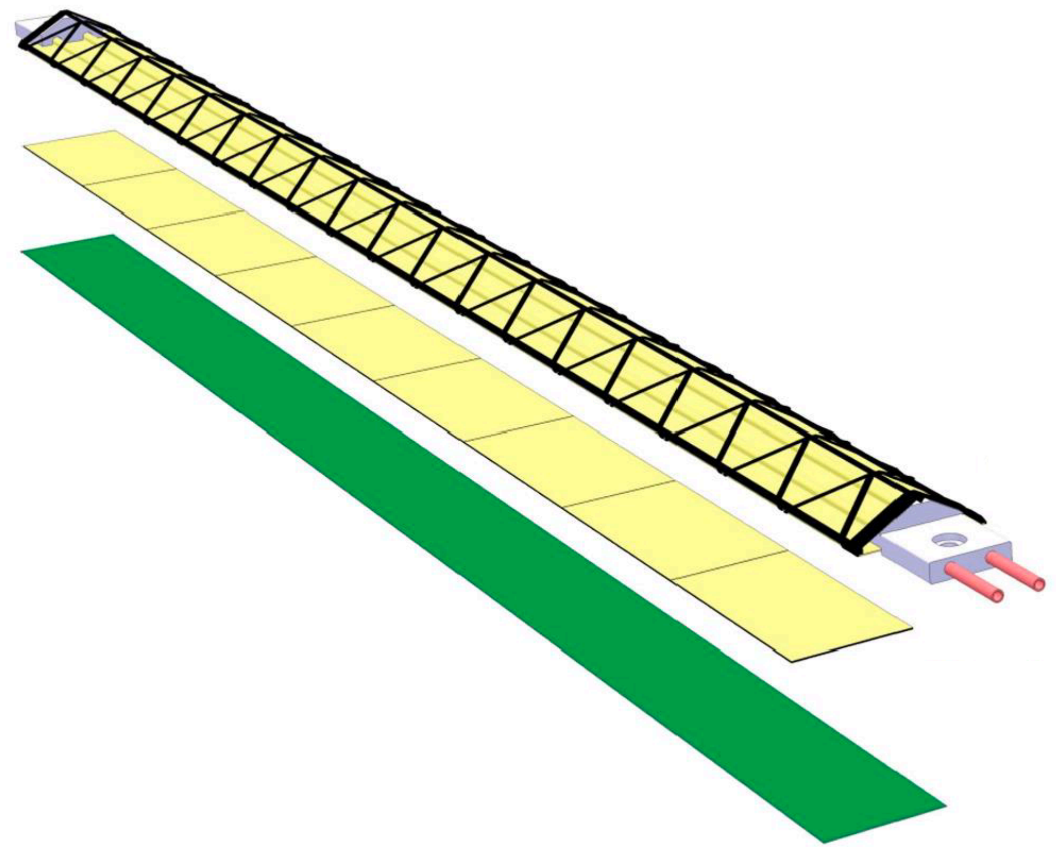




First large-area MAPS-based detectors:
→ traditional staved trackers with reduced material budget and improved resolution

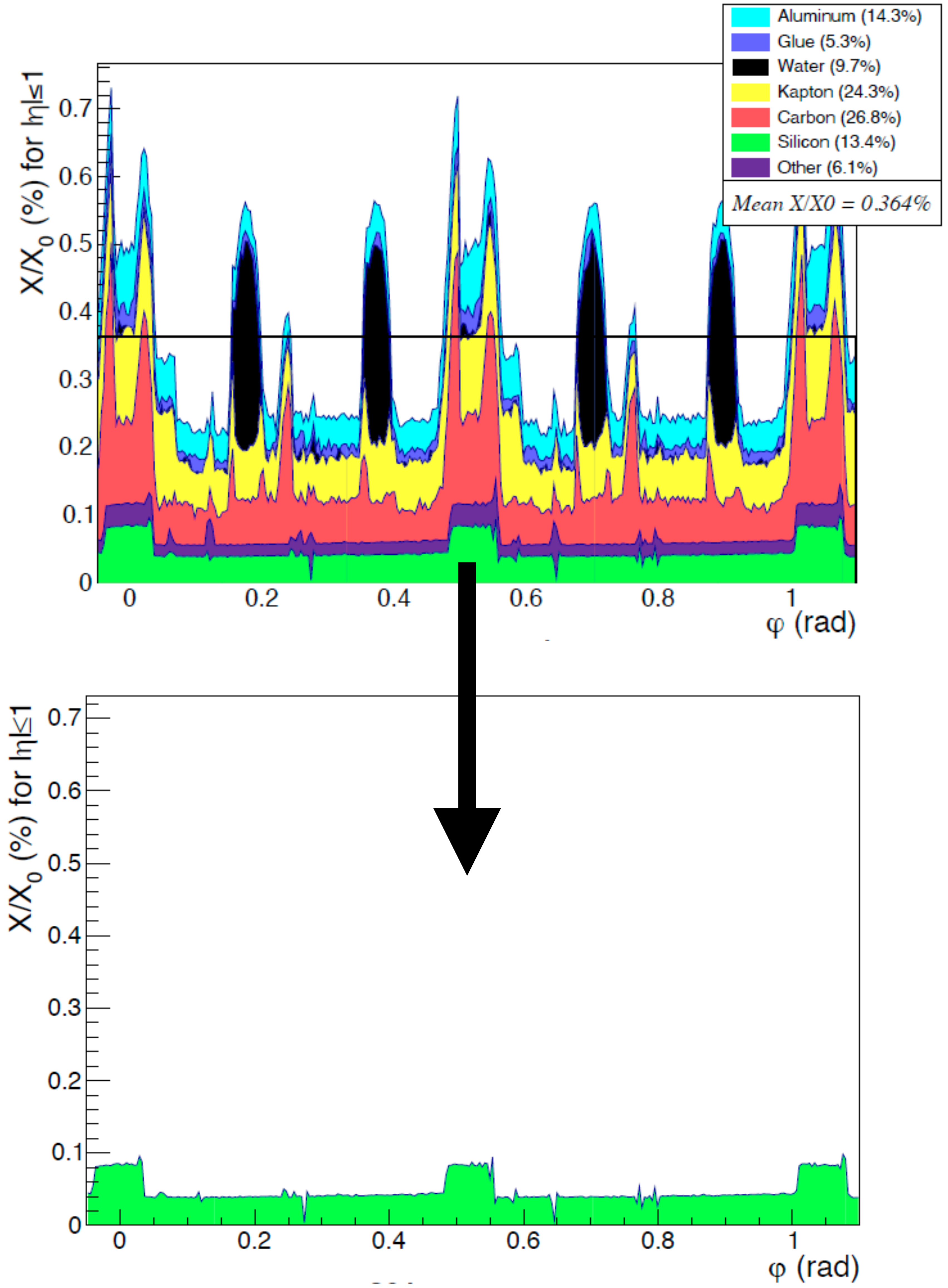
Monolithic Active Pixel Sensors in 180 nm
- Low power consumption heat dissipation
- Thinner/less material
- Commercial process (CMOS)
- Small pixel pitches ~ 10-30 μm

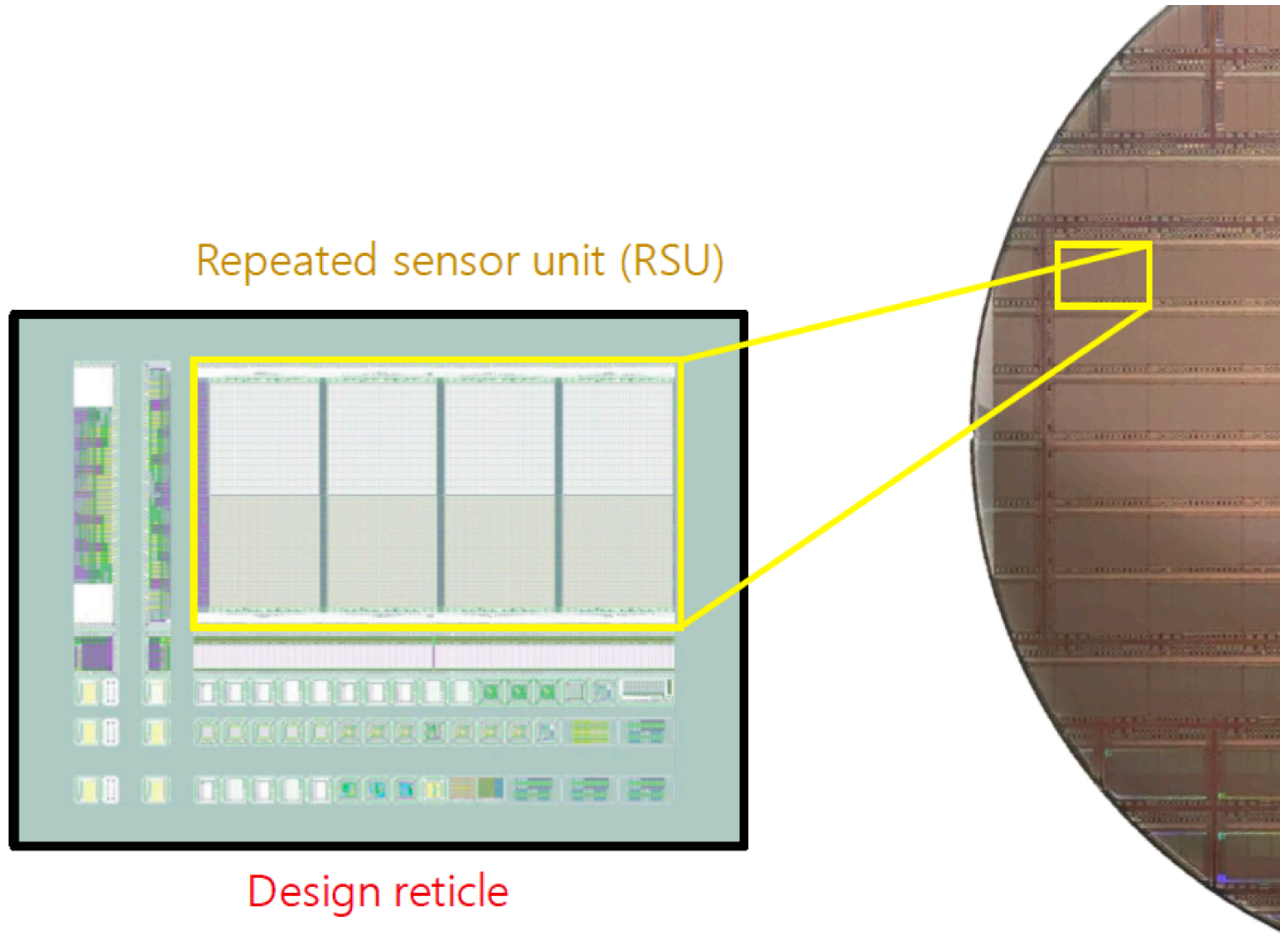




→ ideal choice for very high-resolution trackers for moderate-radiation environment

The new "stitched" ITS3 MAPS technology in 65 nm





With power consumption <40 mW/cm^2
→ **Air-based cooling, no need for liquid-based cooling**

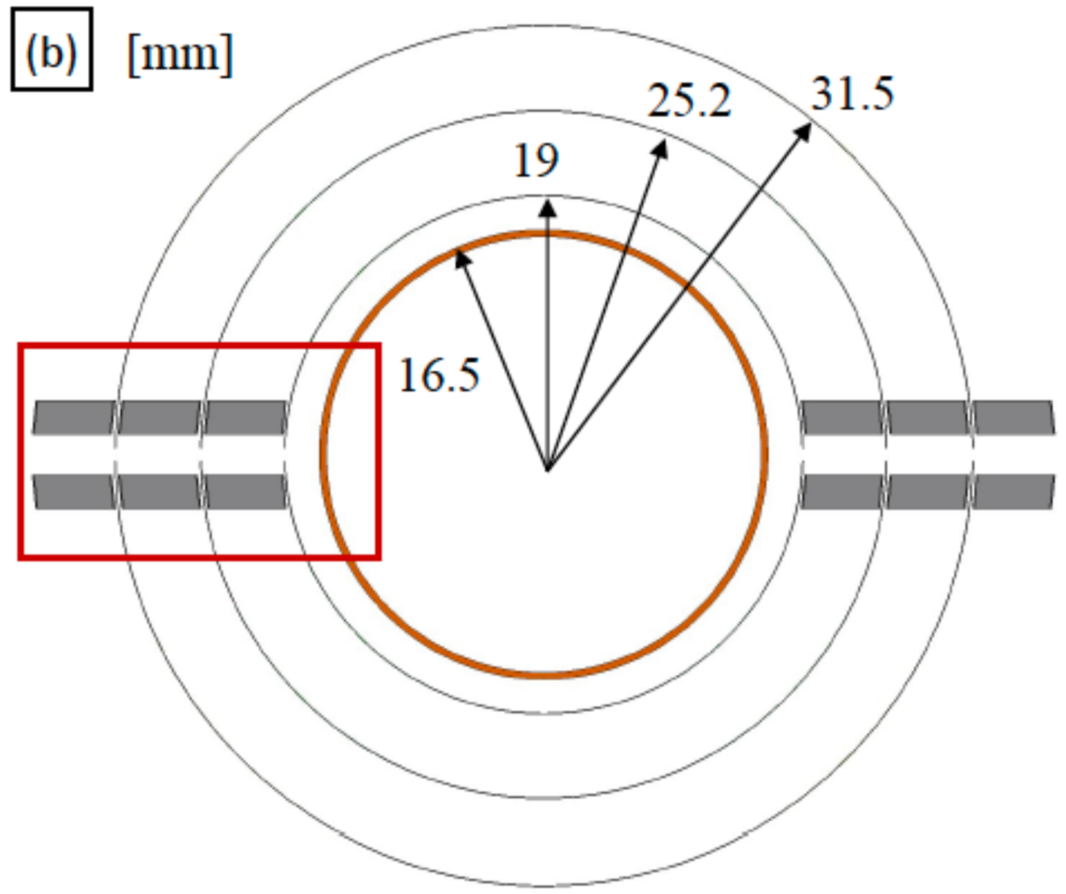
→ **No FPC for data readout and powering**

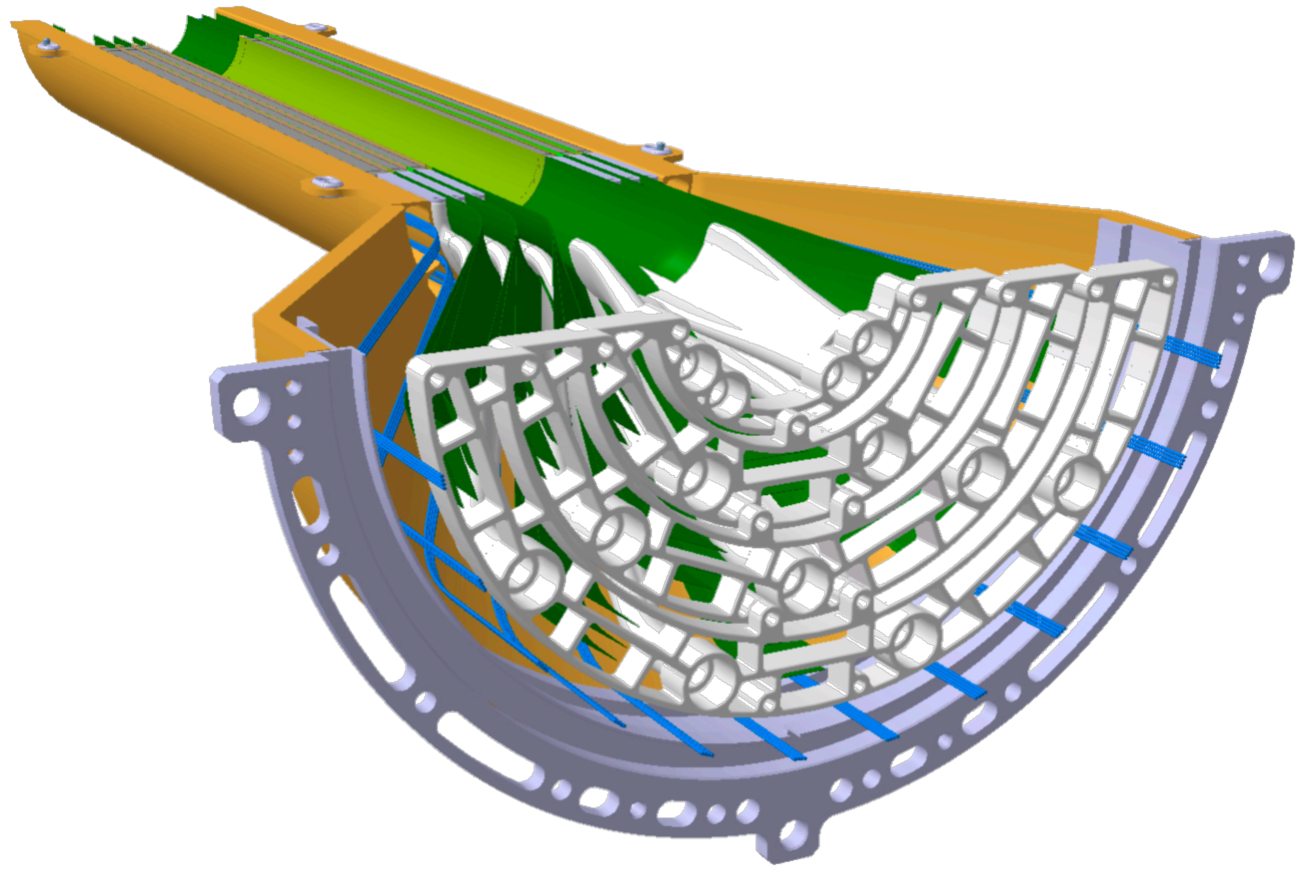
Thanks to the intrinsic stiffness of the curved silicon wafer
→ **Minimal mechanical support**

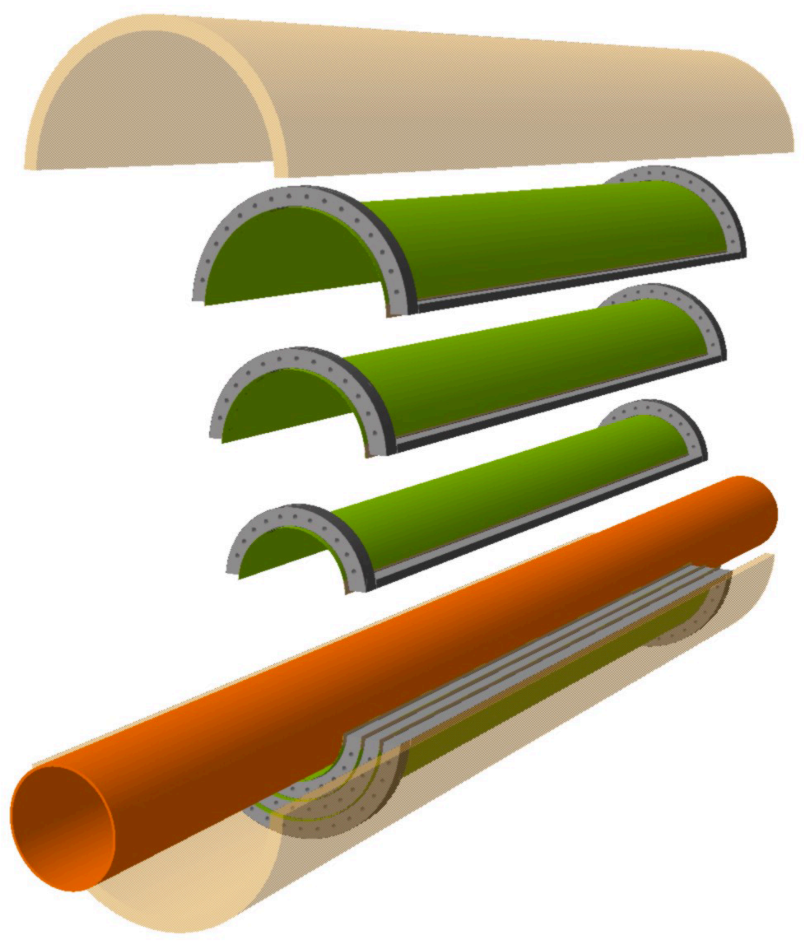
The ITS3 upgrade for ALICE in Run 4

ITS3 upgrade:
- high-occupancy low-interaction rate (PbPb at the LHC)
- only three layers (radii from 1.90 to 3.15 cm)
- small pseudorapidity coverage (no strong constraints on material budget due to services)

Beampipe inner/outer radius (mm)		16.0/16.5	
IB Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	19.0	25.2	31.5
Length (sensitive area) (mm)	260	260	260
Pseudo-rapidity coverage[a]	±2.5	±2.3	±2.0
Active area (cm^2)	305	407	507
Pixel sensors dimensions (mm^2)	266 × 58.7	266 × 78.3	266 × 97.8
Number of pixel sensors / layer		2	
Material budget ($\%X_0$ / layer)		0.07	
Silicon thickness (μm / layer)		≤50	
Pixel size (μm^2)		$O(20 \times 22.5)$	
Power density (mW/cm^2)		40	
NIEL ($1\,MeV\ n_{eq}\ cm^{-2}$)		10^{13}	
TID (kGray)		10	







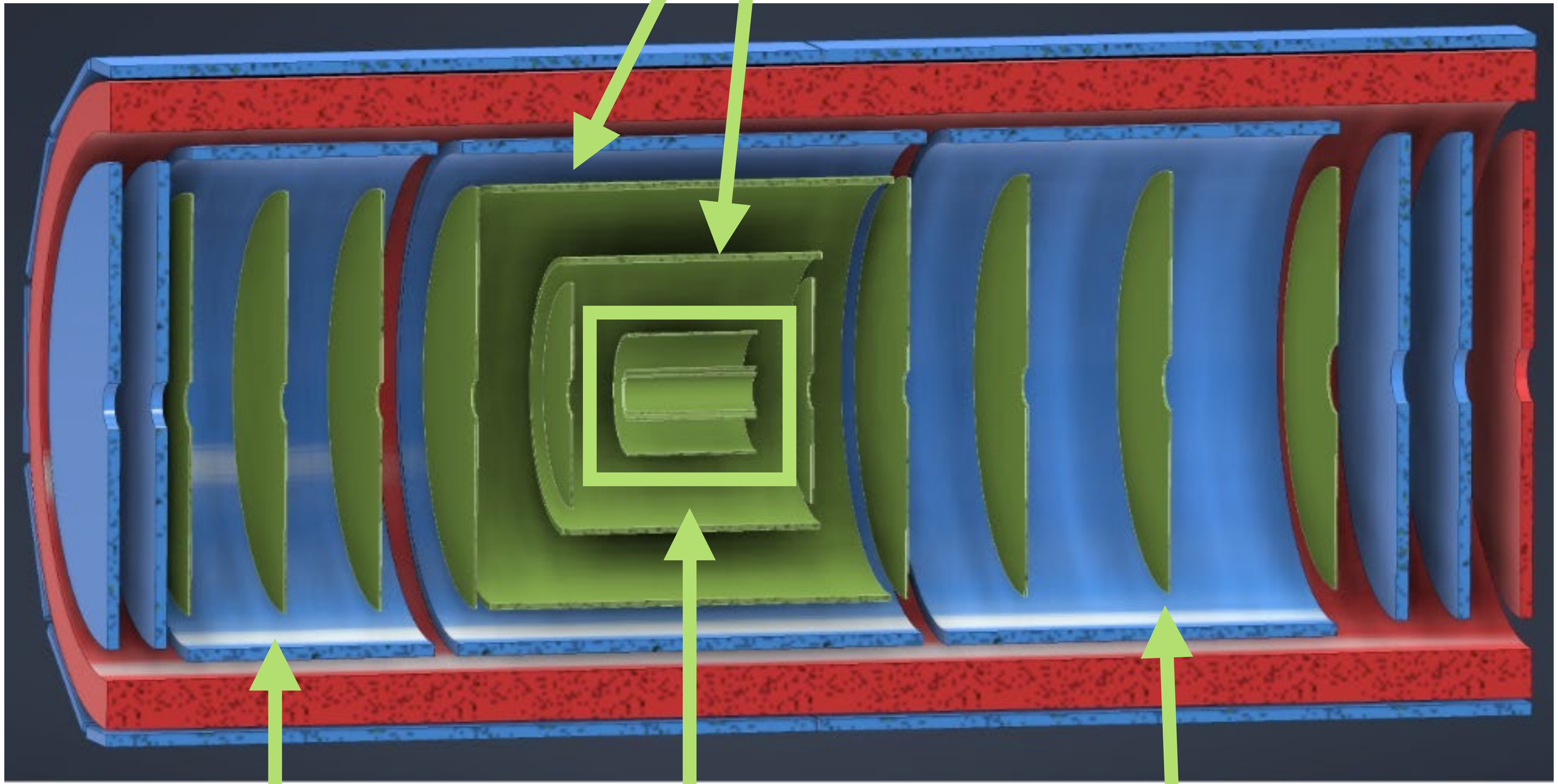
Towards large-area detectors with stitched MAPS: the Silicon Vertex Detector for ePIC

ePIC

The SVT ePIC detector (in green)

SVT outer layers

total area of ~8.5 m²

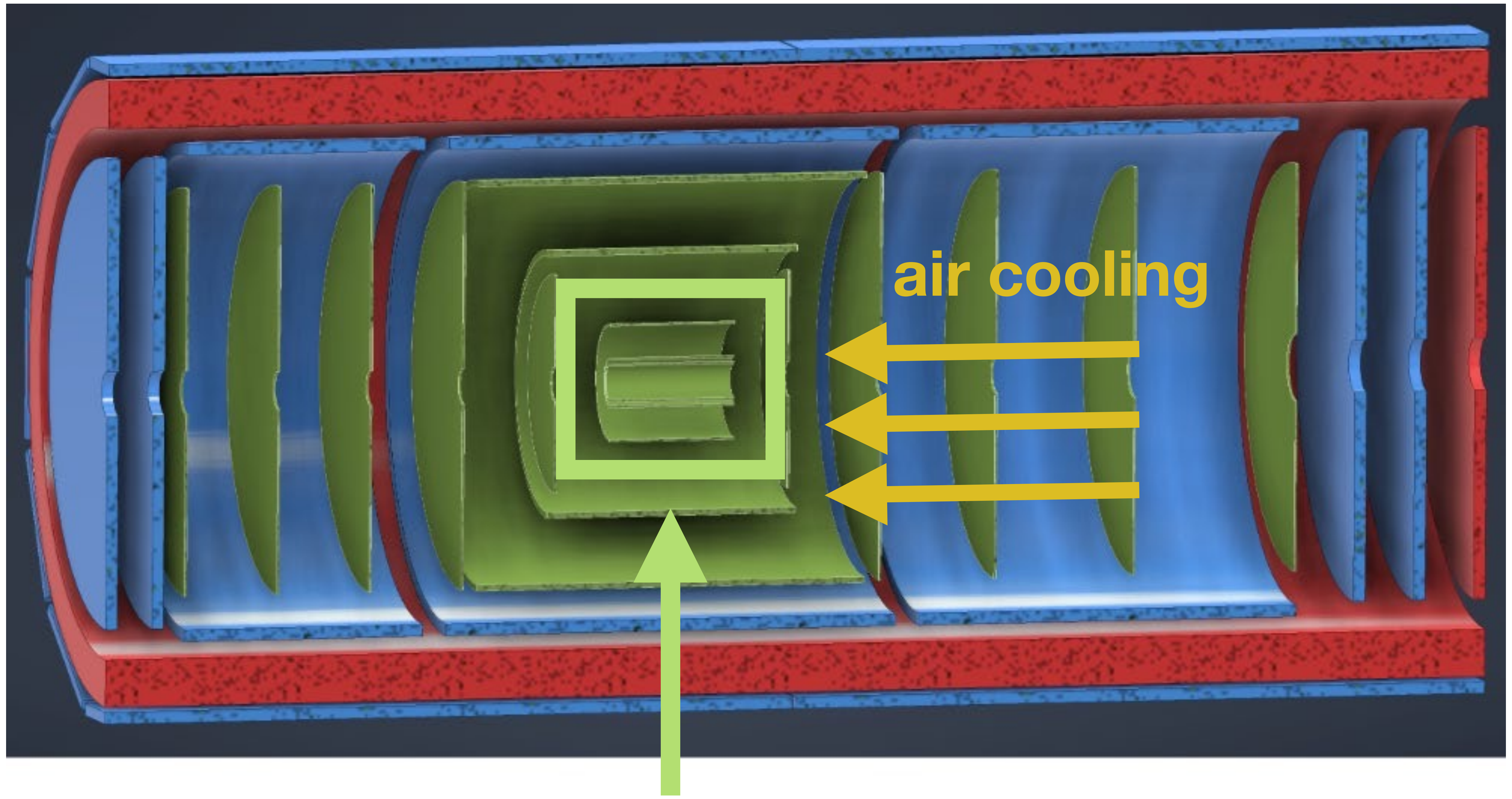


SVT disks

SVT inner barrel

SVT disks

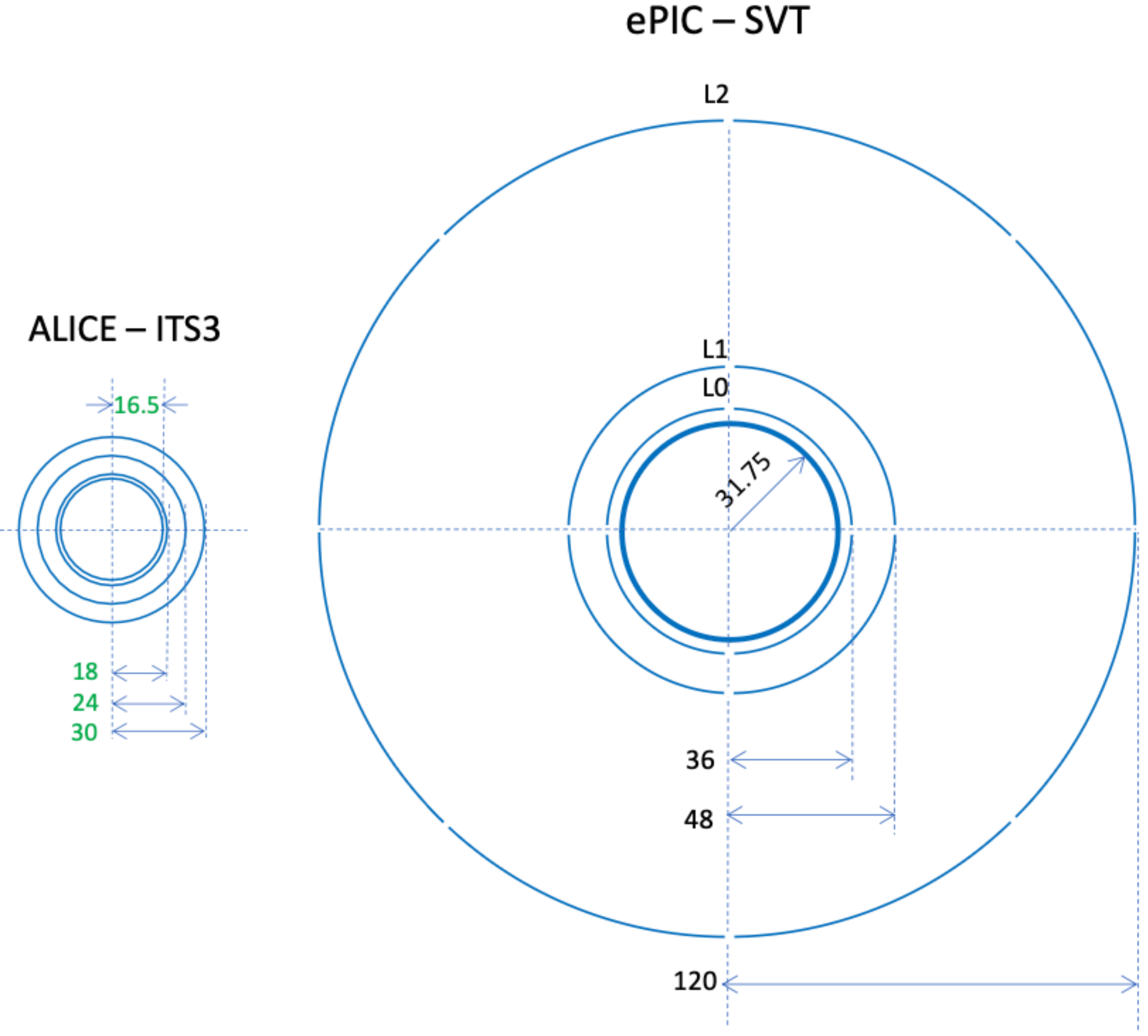
The SVT inner barrel ("bent" layers 0, 1, 2)



SVT inner barrel

- built with **bent ITS3 wafer-size sensors**
- minimal support structure (carbon foam)
- air cooling (~ few m/s)

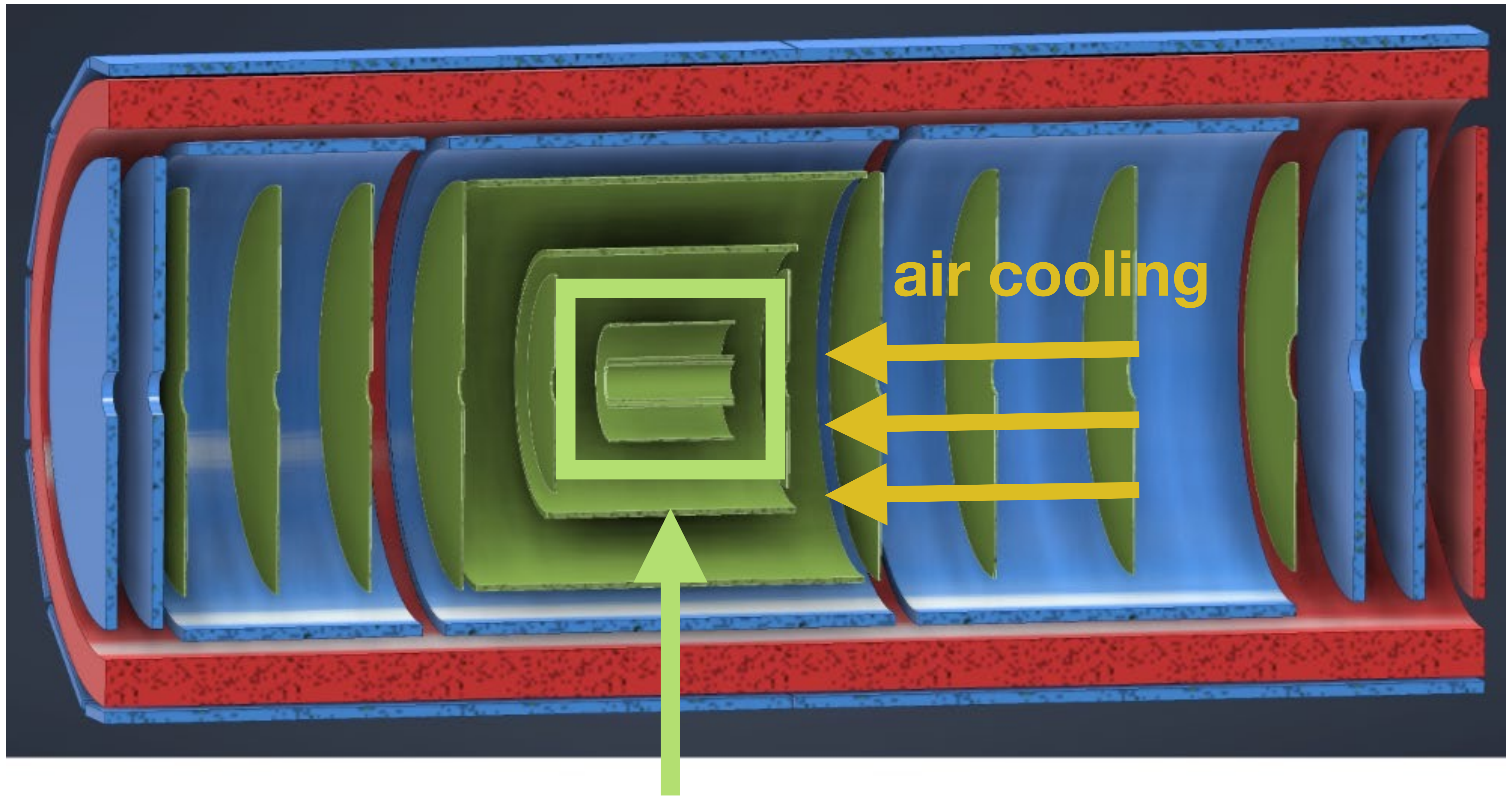
- **Radii = 3.6, 4.8, 12 cm**
- **Lengths = 27 cm**



ePIC specific needs:

- reduce services at forward/backward
- mechanical stability in the presence of a R=12 cm layer (R^{max}_{ITS3} is < 4 cm!)
- air cooling strategy is more challenging due to the presence of the disks

The SVT inner barrel ("bent" layers 0, 1, 2)



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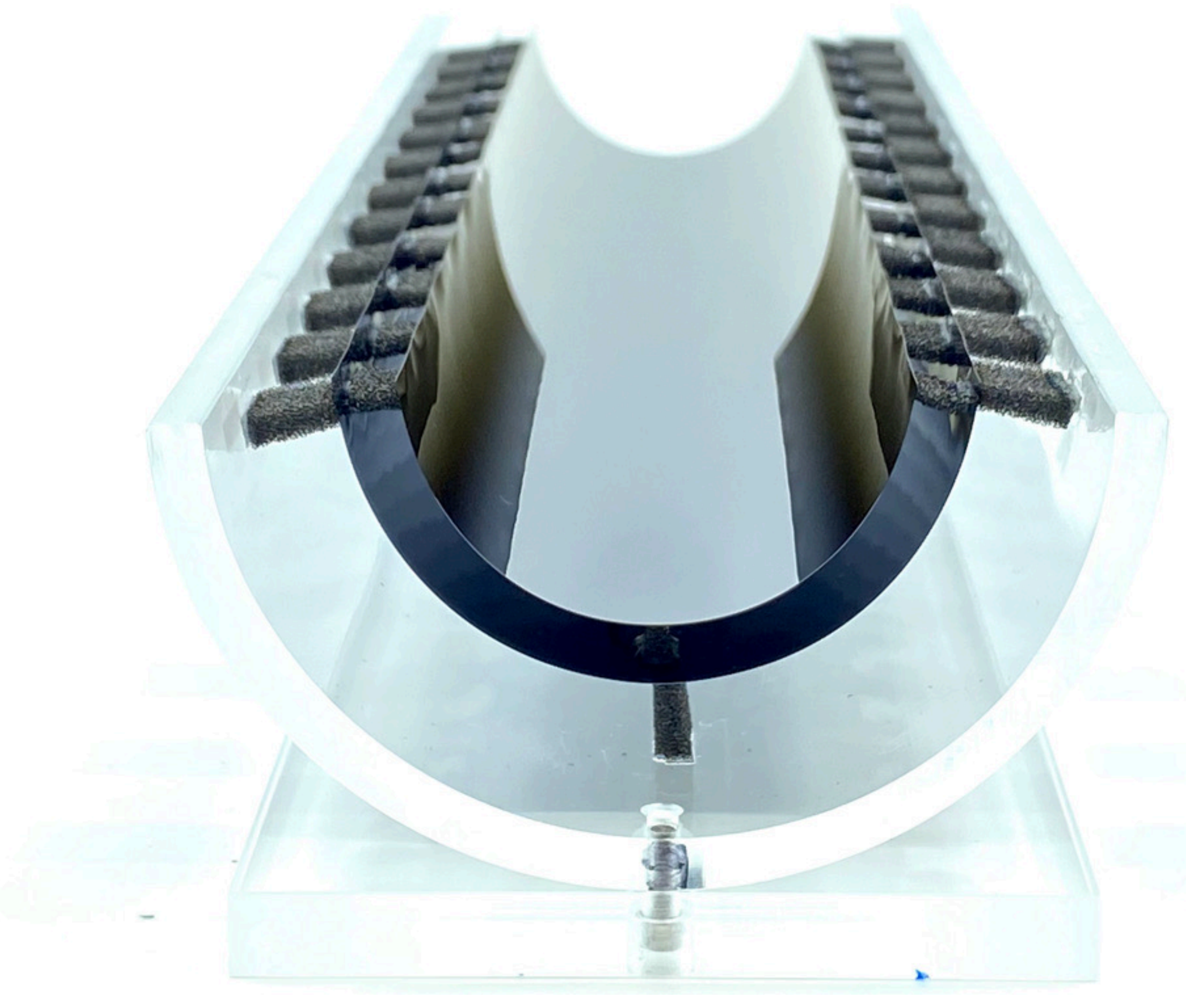

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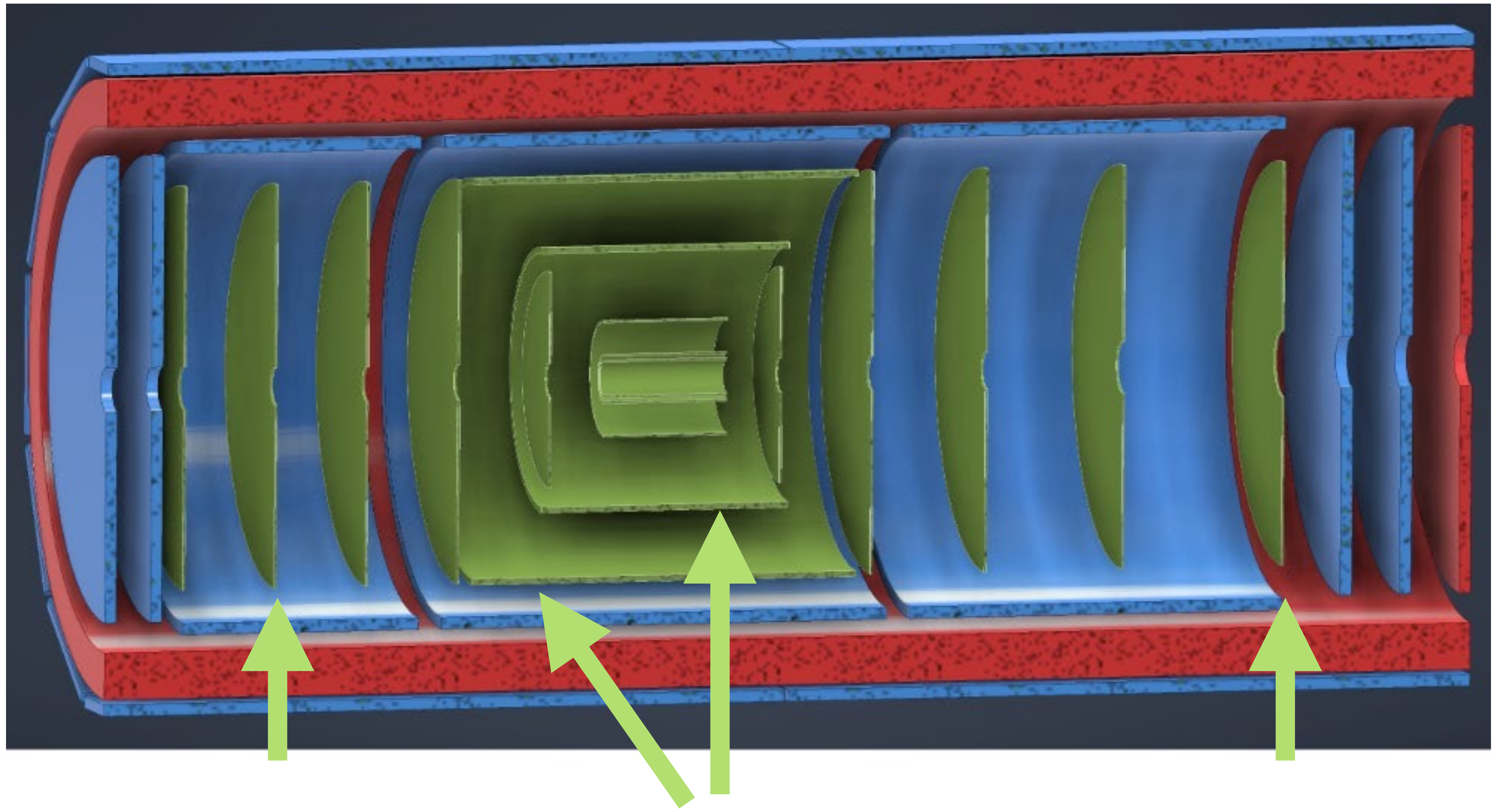
The SVT outer barrel (layers 3, 4) and disks



"Flat" Large Area Sensors (LASs) derived from ITS3 optimised for covering large surfaces

- **traditional staved** structure (not bent)
- carbon fibre support
- integrated cooling (liquid or air)

Challenges:
- preserve the low material budget in the presence of carbon fiber supports and services
- disk geometry can obstruct air cooling for the inner barrel

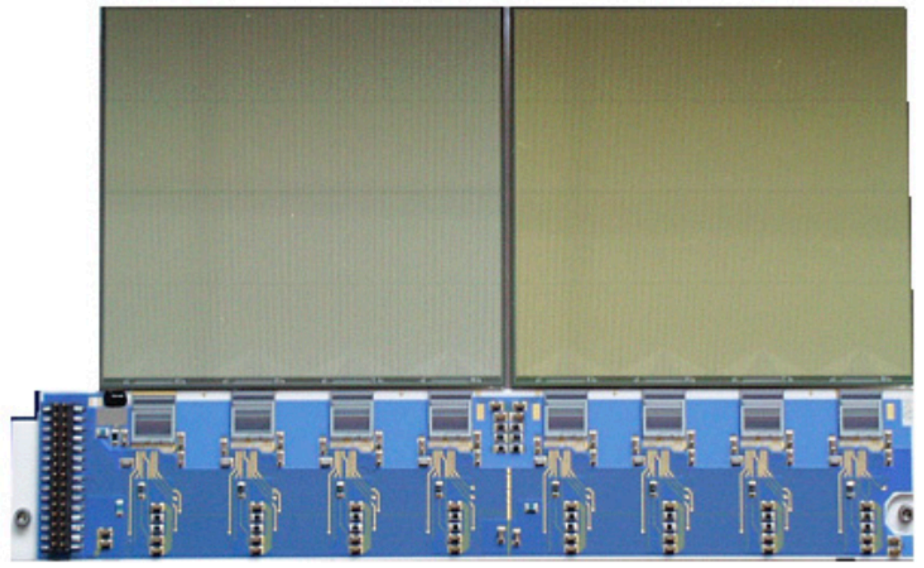
→ **SVT for ePIC** as the most advanced application of stitched MAPS sensors for large-area wide-acceptance detectors
→ **unique benchmark for a future MAPS-based FCC tracker**

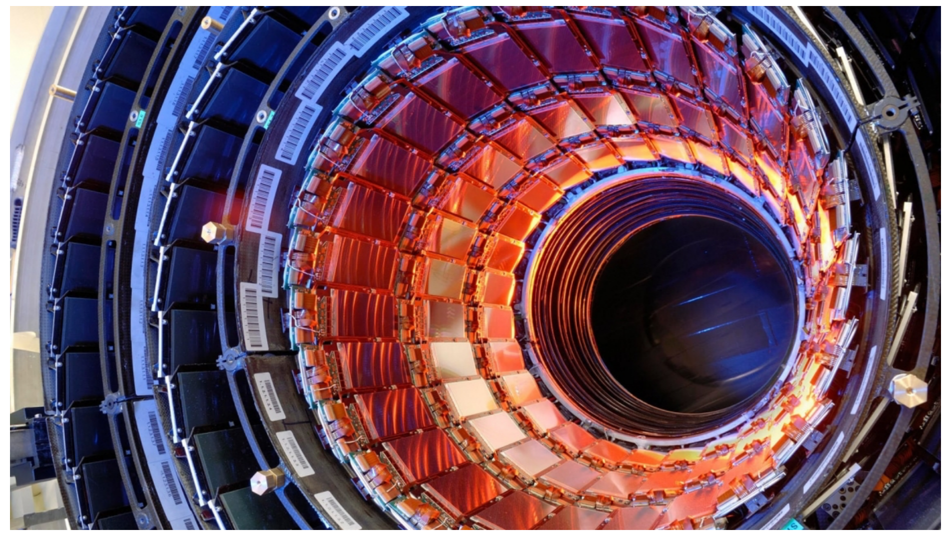
PixELφ lab at MIT

Silicon detectors in the MIT heavy-ion group

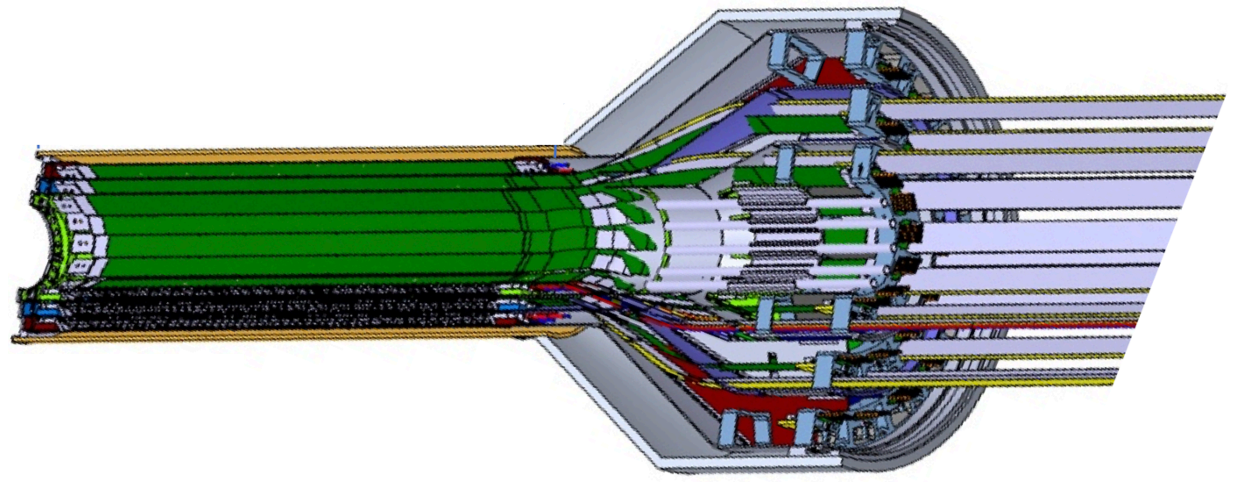
R. Nouicer, B. Wislouch et al., Nucl. Instrum. Meth. A461:143-149, 2001

PHOBOS experiment at RHIC
AC-coupled, single-sided, silicon pad for tracking, vertexing, and multiplicity





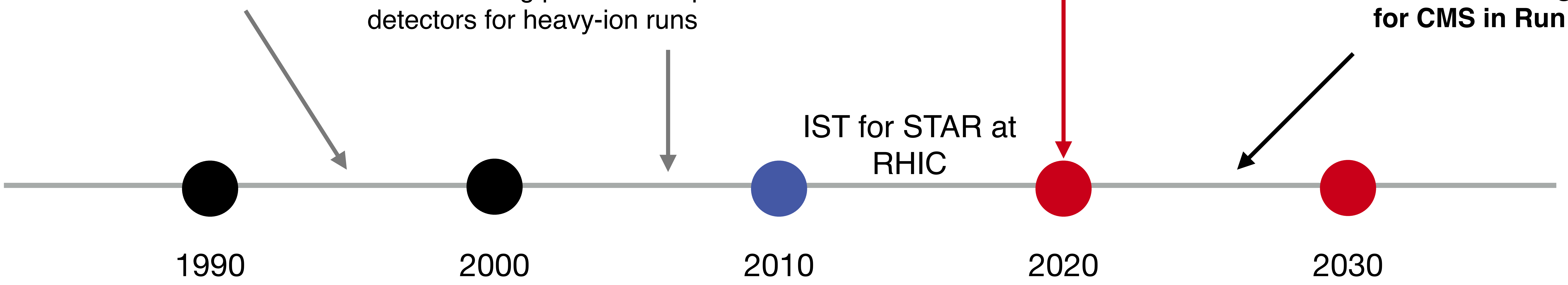
CMS tracker ("hybrid pixels")
commissioning pixel and strip detectors for heavy-ion runs



Monolithic Active Vertex Tracker (MVTX) for sPHENIX with ALICE ITS2 technology

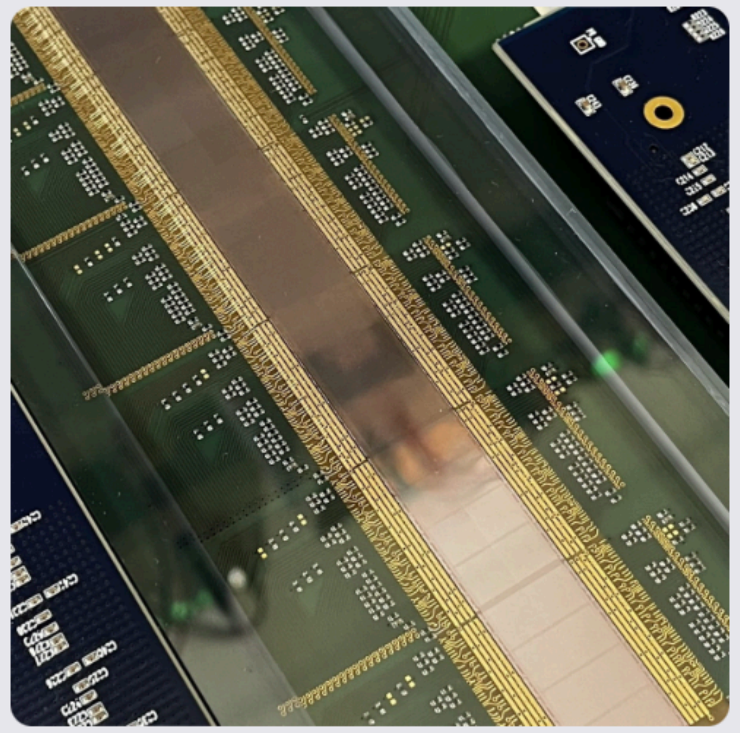
- mechanical design, cooling, and integration
- module characterization
- DCS design, installation and commissioning

Ultra-fast silicon timing detector for CMS in Run 4

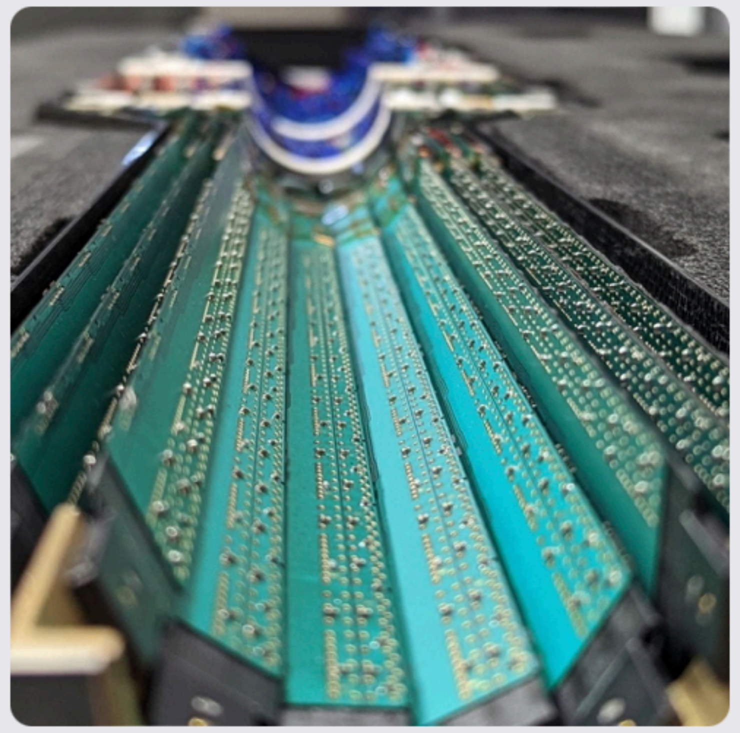


MIT PixELφ : a Silicon Pixel Lab for ELementary physics at MIT

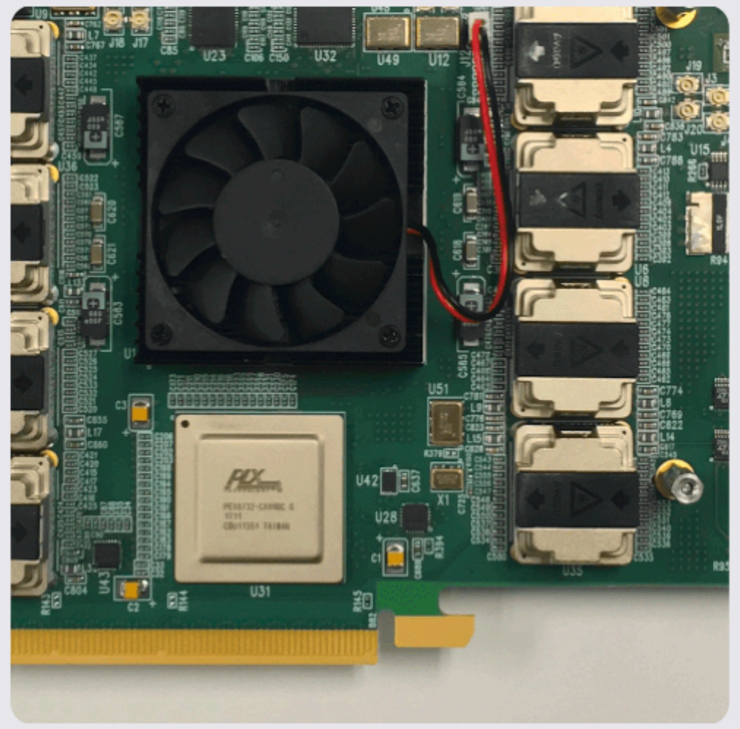
→ **Next generation "stitched" MAPS technology** for high-accuracy detectors for high-energy and nuclear physics



Silicon Vertex Tracker (SVT) for the ePIC experiment at the Electron-Ion Collider



MVTX for the sPHENIX experiment



Artificial intelligence with FPGA for MAPS detectors

Key strategy for the SVT project:

→ **short term:** build a CERN-based MIT pixel lab to maximize synergies with the R&D for ALICE ITS3

→ **middle-long term:** MIT as a leading institute to exploit next-generation MAPS for particle physics

Overview of the R&D phases of the ITS3/SVT sensors

Stitched bent sensors for ITS3 and first three layers of the SVT

MLR1: qualification of CMOS 65nm technology, prototype for circuit blocks

ER1: stitching technology demonstrator (MOSS and MOST sensor), yield studies

ER2: fully functional sensor that satisfy ITS3 requirements

ER3: final production and design (bug fixes from ER2)

Stitched flat sensors for the outer layers of the SVT detector:

Large Area Sensor (11): stitched “flat” larger area sensor

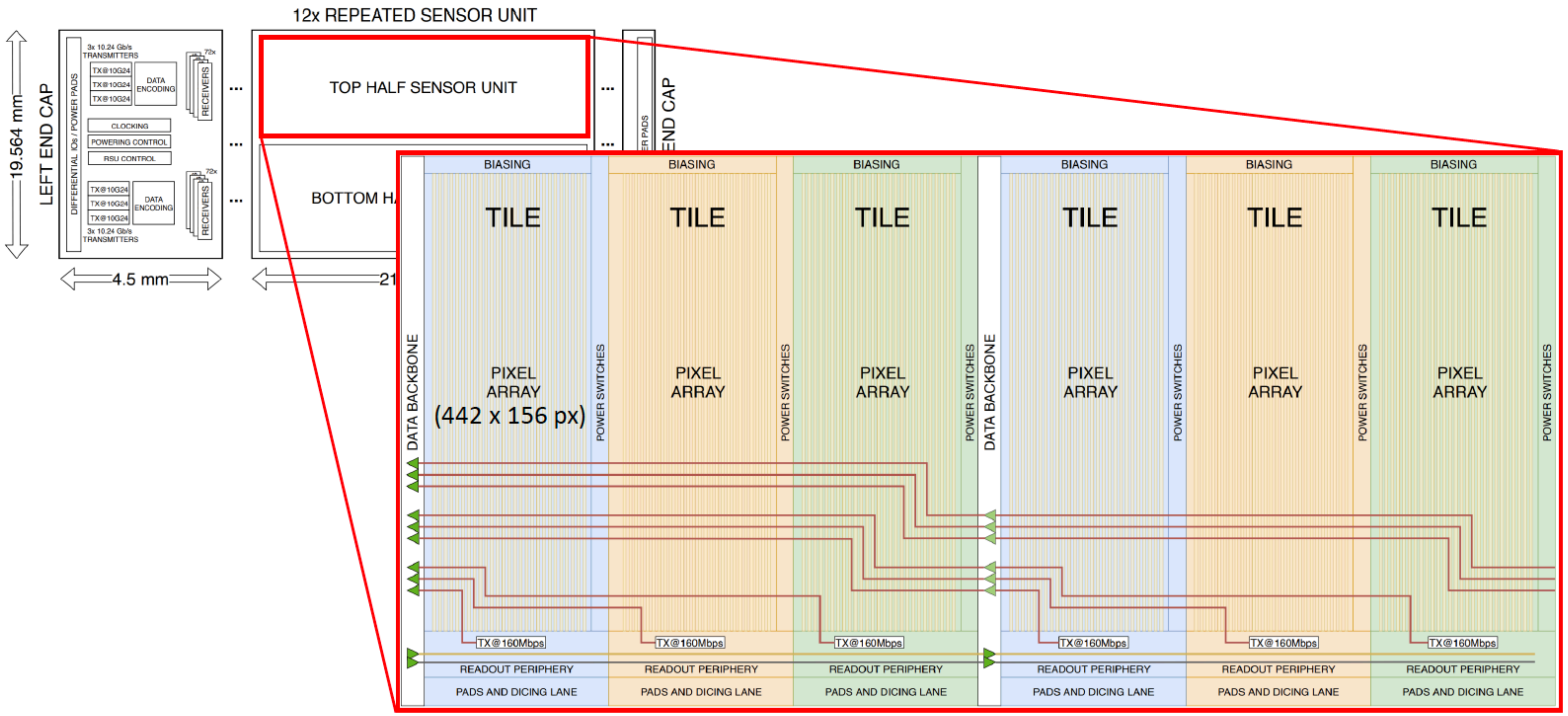
SVT at the ePIC: timescale and synergies with the ITS3 project

Key strategy of MIT PixELphi lab for the SVT project:

- build a CERN-based MIT pixel lab to maximize synergies with the R&D for ALICE ITS3 for ER2/ER3
- specific R&D for SVT detector (focus on data and service reduction)

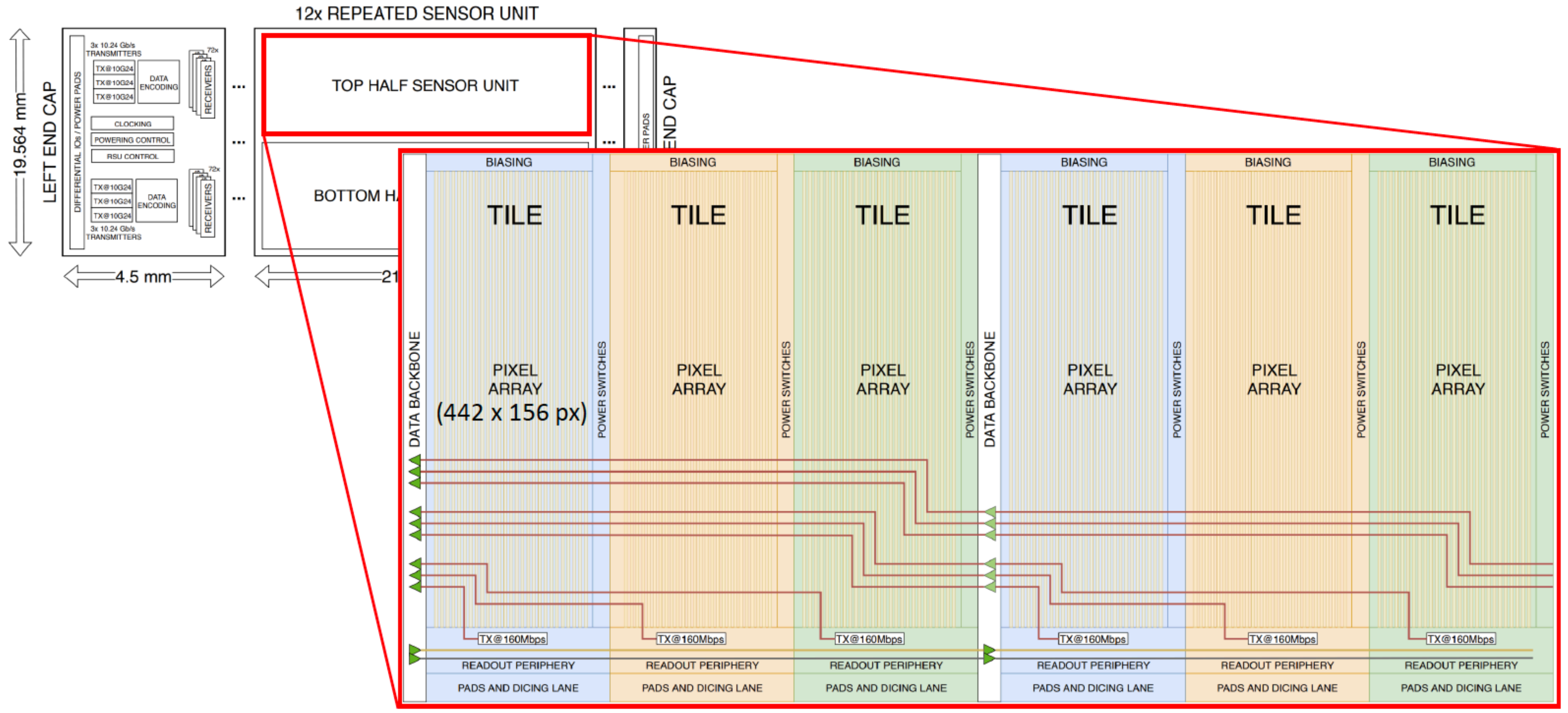
MIT PixELφ lab for the SVT: sensor design

Sensor design for ER2/ER3 (MIT engineer working in the CERN micro-electronic department)
• digital design, test, and signoff of the Engineering Run 2/3
• development and implementation of digital blocks in the Repeated Stitched Units (RSU) and Left End-Cap (LEC) of the ITS3 sensor



MIT PixELφ lab for the SVT: sensor test and readout R&D

Developing a new testing system to perform high-frequency tests on MAPS using a wafer probe setup
• development of the ER2 test system with probe cards, adapter cards, and software that will automate pixel matrix scans
→ **coordinating the SVT working group on sensor testing and characterization**



• **Challenges**: high-frequency, low impedance with very thin sensors
→ **crucial R&D to exploit stitched sensors for large-area detectors**

New 12 inches machine acquired by MIT PixELφ
→ optimized for testing of thin wafter

MIT PixELφ lab for the SVT: sensor test and readout R&D

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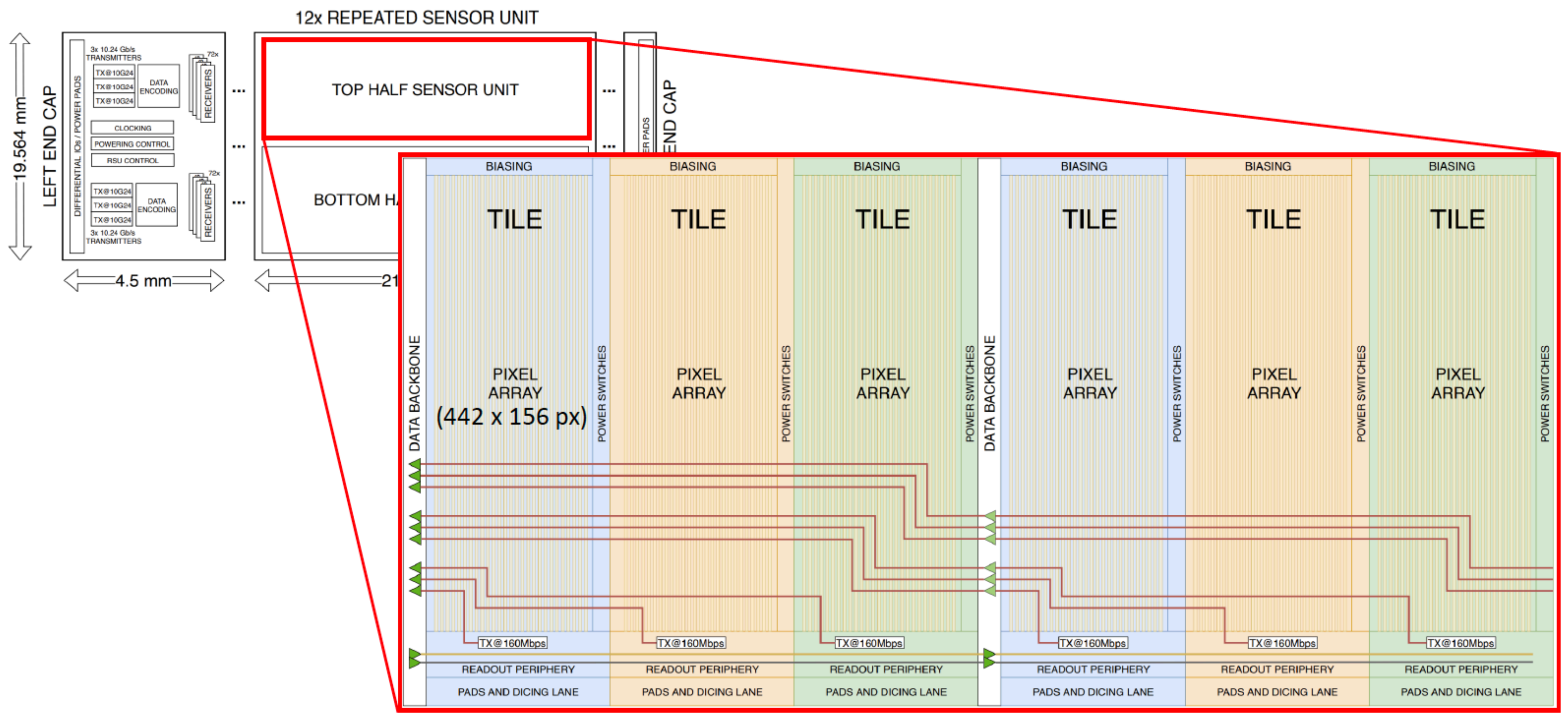
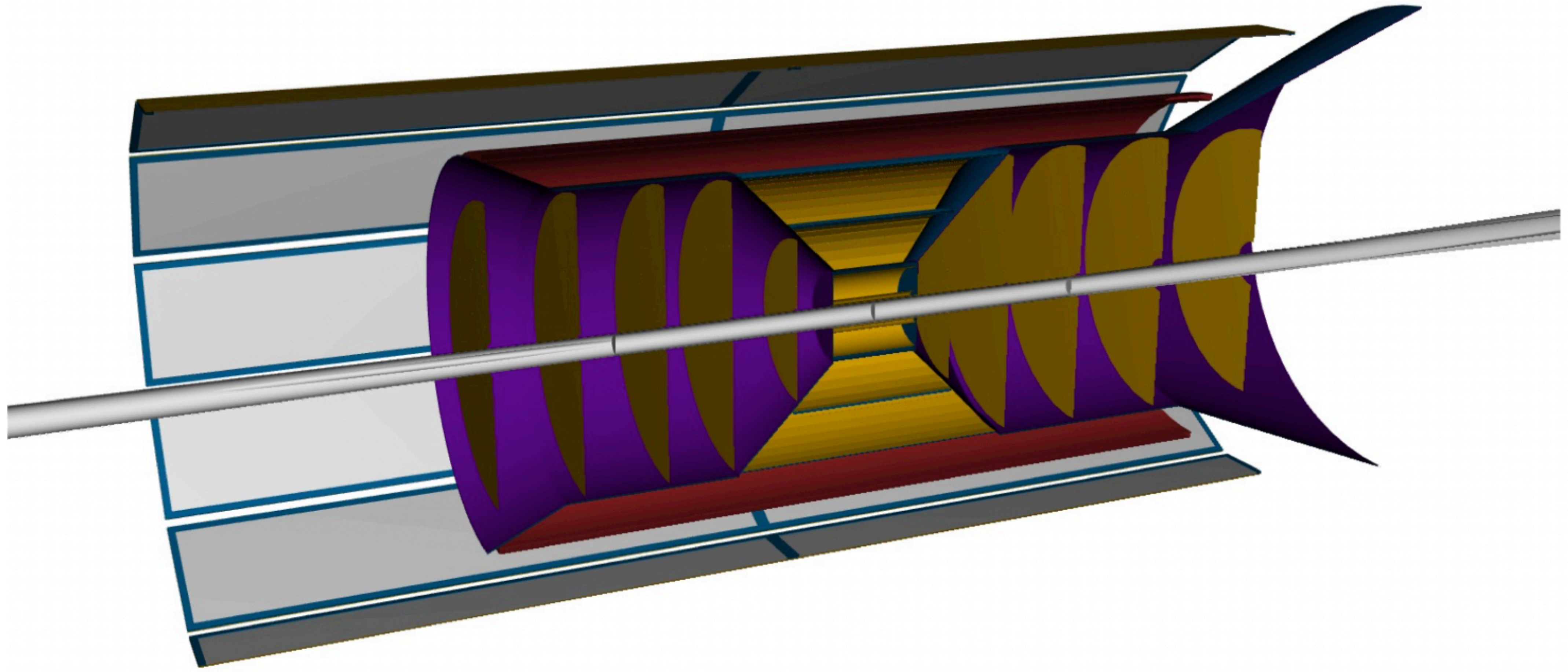


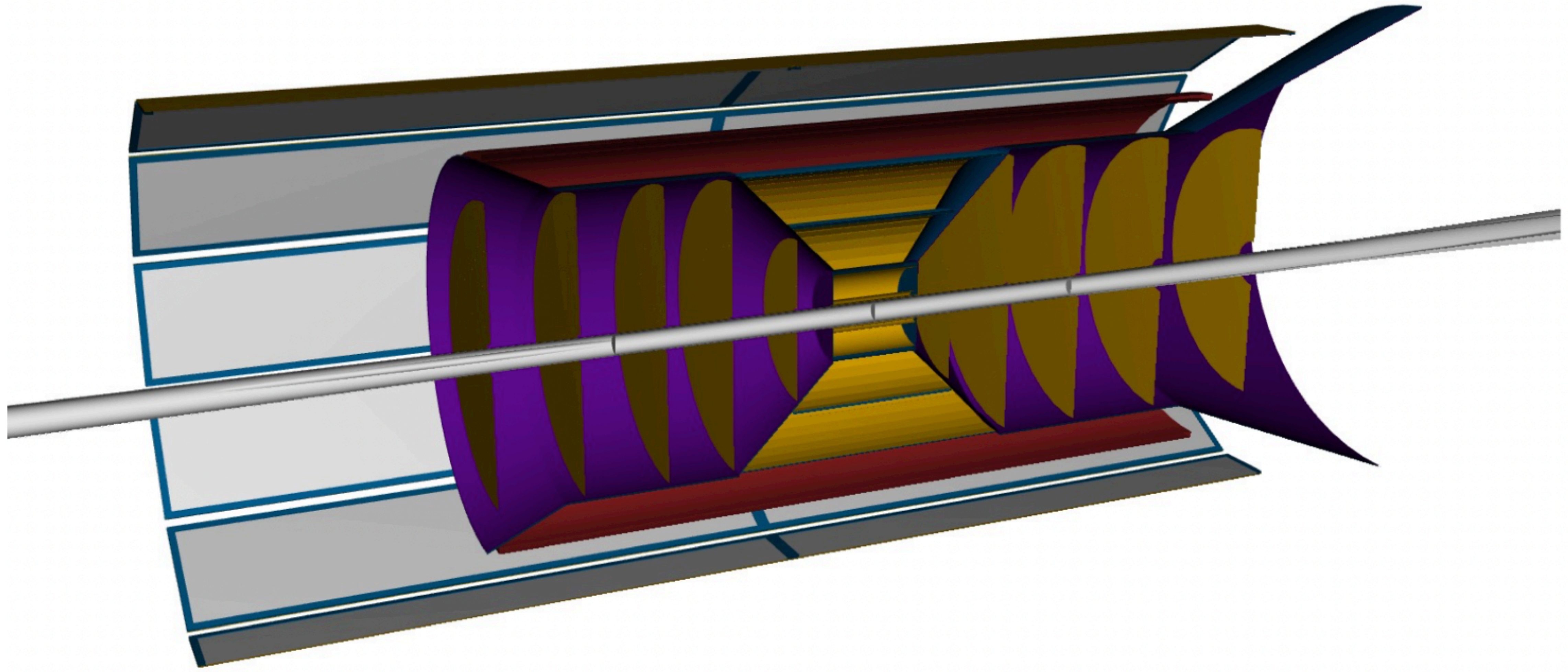


Design and optimize the SVT readout strategy for service reduction

- multiplexing strategy for the output links of the EIC LAS with FPGA-based technologies (short term) and with AI on MAPS

Conclusions

New lab PixELphi to exploit new generation MAPS for high-energy and nuclear physics



Key role in the R&D for the new MAPS sensors for SVT tracker at EIC
→ ongoing effort on sensor design,
readout R&D, and R&D for new testing strategies for large MAPS

Long-term focus: exploit and develop MAPS for large-area large-η detectors
→ **clear synergy with the R&D for a future FCC tracker**

Thank you very much for your attention!

→ Please get in touch if you are interested in collaborating with us! https://pixelphilab.mit.edu

BACKUP